Modelling and fabrication of high performance Schottky-barrier SOI-MOSFETs with low effective Schottky barriers

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Chapter 1

Introduction

Since the advent of CMOS technology, the semiconductor industry has been successful in achieving continuously improved performance. The feature size of the most important electronic device, the metal-oxide-semiconductor field-effect transistor (MOSFET), has already been reduced from about 10 μm to the sub-100 nm regime during the last 30 years. The enormous miniaturization and integration of MOSFET devices has made possible a dramatic development in microelectronics. The so-called Moore's law, formulated in the 1960s, states that the transistor number on an integrated circuit chip doubles every 18 months and predicts that the characteristic feature size will be in the 30 nm regime by the year 2015. But according to the 2003 ITRS road-map [1], the 30 nm feature size will be reached much earlier than expected because of an accelerated device scaling. However, technological as well as fundamental limits are being reached soon due to different issues associated with increasing source/drain (S/D) parasitic resistance, excessive gate oxide leakage and deteriorated device performance due to short channel effects (SCE). These issues force the semiconductor industry to consider substantial changes regarding device technologies and different architectures such as Schottky barrier (SB)-MOSFETs or multi-gate MOSFETs as well as the integration of novel materials such as high-k [2] dielectrics as gate material, Si on insulator (SOI) [3] or strained silicon [4] as channel materials. SOI is already believed to be the standard material to replace bulk-Si for next generation devices because of its advantages in terms of preserving the electrostatic integrity in aggressively scaled devices [5, 6]. The choice of the SB-MOSFET structure is due to its metallic S/D electrodes with low specific resistivity, high scalability even down to the sub-10 nm regime and good process compatibility with current standard Si technology [7, 8]. Hence, the SB-MOSFET architecture provides solutions to some of the critical road-map challenges.

A self-aligned silicide process is usually employed to create silicide source-drain contacts. Silicides are also an excellent choice to realize metallic source and drain electrodes [9]. However, for typical SB-MOSFETs, the on-current is always limited by the existence of the SB at the S/D contact and thus the performance of SB-MOSFETs is still not comparable with conventional MOSFETs with highly doped S/D. Therefore, finding an appropriate material with a low Schottky barrier height (SBH) is required in order to improve the performance of SB-MOSFETs. Among the different silicides investigated as gate, S/D contact material, NiSi is believed to be promising to be incorporated into future advanced conventional MOSFET devices because of its low specific resistivity and high scalability [10, 11, 12]. However, the high SB (0.64eV on n-Si) hinders its application in SB-MOSFETs. While platinum silicide [13, 14, 15], erbium silicide [16, 17] or ytterbium silicide [18] provide reasonably low SBH for p and n-type devices, problems with thermal stability and scalability of these materials in the process integration limit a wider use.

In order to take advantage of the SB-MOSFET architecture and NiSi, SB engineering is needed. Therefore, the focus of this thesis is to improve the electrical performance of fully nickel silicided SB-MOSFET devices on SOI. Simulations are performed to study the impact of the gate oxide (t_{ox}) and channel thickness (t_{si}) on the performance of SB-MOSFETs. In addition, the effect of silicidation induced dopant segregation (DS) on the effective SBH will be investigated. The electrical behavior of experimental SOI SB-MOSFETs confirms what is observed in the simulations: The use of ultra-thin gate oxides and ultra-thin channels in combination with the formation of a thin, highly doped layer at the silicide/Si interface significantly improves the on- as well as the off-state of the devices. This improvement stems from a significant lowering of the effective SBH. As a result, an effective SBH as low as $\sim$0.1eV for electrons can be achieved in a device with $\sim$3.7nm gate oxide and $\sim$25nm channel thickness and a few nanometer thin highly doped layer at the fully silicided S/D and thus provides an alternative way to relax the requirement of low Schottky barrier silicide materials for high performance SB transistor devices.

This thesis is organized as follows: In chapter 2, the basic principles of Schottky diodes and SB-MOSFETs are given. Chapter 3 introduces the material characteristics of nickel silicide and concentrates on the effect of silicidation induced dopant segregation. Chapter 4 is dedicated to the investigation of the impact of geometrical parameters and dopant segregation on the electrical behavior of SB-MOSFET by simulations. Diodes with and without dopant segregation are investigated in Chapter 5. The detailed fabrication process of long- as well as short- channel SB-MOSFETs is introduced in chap-

ter 6. Chapter 7 presents the experimental results of fabricated devices and analyzes the factors affecting the electrical performance of SB-MOSFETs.

Chapter 2

Principles of SB-MOSFETs

2.1 The SB-MOSFET

With the down-scaling of transistor gate length, junction depth of source/drain extensions must be scaled down at the same time in order to suppress short channel effects (SCE). However, for conventional MOSFETs as shown in Fig. 2.1(a), the formation of ultra-shallow junctions requires ultra-low energy ion implantation and dopant diffusion caused by high temperature annealing must be avoided in order to get a high scalability and a low resistance of the source/drain extensions. This is a major challenge for current processing technology. In contrast, the structure of SB-MOSFETs as shown in Fig. 2.1(b) is composed of a silicide source and drain. This means that Schottky contacts replace the p-n junctions. Compared to a p-n diode, the Schottky diode exhibits a larger leakage and it is rather difficult to fabricate reproducibly since the Schottky barrier height (SBH) is very sensitive to small process fluctuations. Nevertheless, this unique change in structure offers many advantages such as:

- an atomically abrupt junction: The ultra-shallow junction can be formed easily and accurately, since the silicided junction depth is controlled by the deposited metal thickness and the thermal budget, yielding a high potential scalability.

- reduced parasitic source/drain resistances: The silicide has a much lower specific sheet resistance than highly doped source/drain extensions.

- low thermal budget and simple processing: This allows the integration of a high-k gate insulator and a metal-gate.

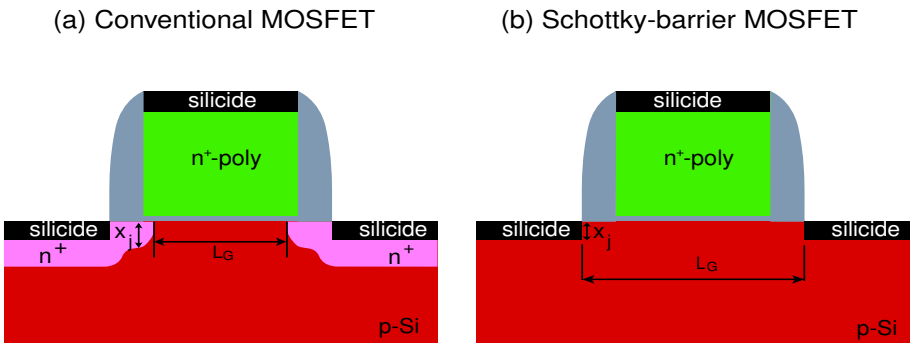


Figure 2.1: Schematic cross-section of (a) a conventional MOSFET and (b) a Schottky-barrier MOSFET.

- no need for channel doping: Because of the existence of a SB at the contact channel interface, channel doping can be avoided. In turn, a lower channel doping leads to reduced scattering of carriers in the channel.

Based on the advantages mentioned above, SB-MOSFETs have been proposed as an alternative to conventional MOSFETs for sub-100nm applications and have received an increasing attention in recent years because of the dramatic down-scaling requirement of transistor devices. Simulations have already shown that the SB-MOSFET can be well scaled down to the 10 nm gate length regime [7]. However, drawbacks of SB-MOSFETs are mainly due to the potential barrier between the metal contact and the channel resulting in lower on-currents and a poor subthreshold behavior compared to conventional MOSFETs. Although intensive research has been devoted to low SBH contact materials such as rare earth silicides $ErSi_2$ or $YbSi_2$, and PtSi with reasonably low SB for n-type and p-type devices, SB-MOSFETs still do not reach the best intrinsic $I_{on} - I_{off}$ performance achievable in conventional MOSFETs with highly doped source/drain contacts. In addition, the problems of stability and scalability of rare earth materials in the process integration impede its wider use. Before we will explore the concept of the SB-MOSFET in more detail, the metal-oxide semiconductor capacitor will be illuminated since the MOS capacitor is at the heart of the transistor and a good understanding of its behavior is indispensable for finding solutions to the problem associated with scalings.

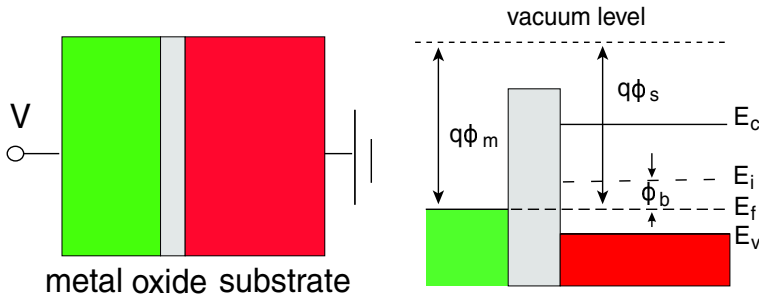


Figure 2.2: The MOS capacitor.

2.2 The MOS-capacitor

In this part, a short introduction to the MOS capacitor will be presented. A detailed explanation can be found in Ref. [19]. The cross-section of a MOS capacitor, shown in Fig. 2.2, consists of a p- or n-type silicon substrate covered with an insulating layer. In most cases, this insulator is silicon dioxide. The conducting layer on top of the insulator is called the gate. An ideal energy band diagram of the three components with zero bias is shown in Fig. 2.2. The Fermi level of silicon and the metal is at the same height. For intrinsic silicon, the Fermi level E_f lies approximately in the middle of the band-gap. Dependent on the type of doping, acceptor or donator, and the doping concentration, the Fermi level E_f will be away from the intrinsic Fermi level E_i by the amount ϕ_b, which is given by the following equation for a non-degenerate semiconductor.

$$q\phi_b = E_i - E_f = \pm kT \cdot \ln \frac{N_b}{n_i}, \tag{2.1}$$

where the $'+'$ sign applies for p-type and the $'-'$ for n-type silicon, respectively. Here, q is the electron charge, N_b is the bulk dopant concentration, n_i is the intrinsic carrier density ($1.4 \cdot 10^{10} cm^{-3}$ in case of silicon) and T is the absolute temperature. If the silicon is degenerate, the Fermi level is within a few kT ($\sim 3kT$) of the conduction or valence band edge. With an external voltage V_g applied to the MOS capacitor as shown in Fig. 2.3, the gate voltage drop across the capacitor can be written as the sum of V_{ox} across the oxide, the surface potential ϕ_s directly beneath the oxide silicon interface, and the work function difference between the gate and the bulk, identified as Φ_{ms}. Thus,

$$V_g = V_{ox} + \phi_s + \Phi_{ms}. \tag{2.2}$$

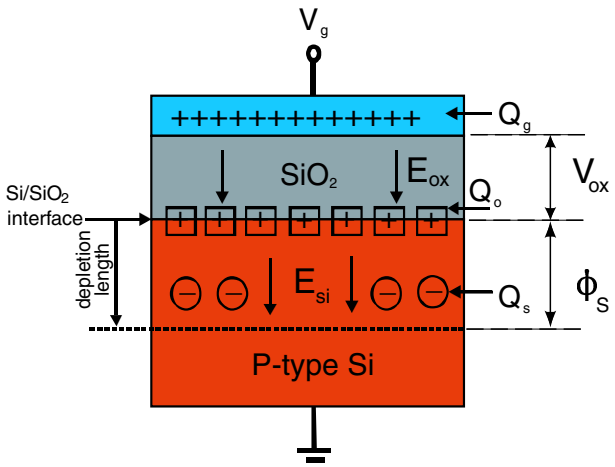


Figure 2.3: MOS capacitor under a positive applied gate voltage V_g showing charges, fields and potentials.

The induced charge on the gate (Q_g), the effective interface charge at the interface between the oxide and the silicon (Q_o) and the depletion charge (Q_s) in the silicon meet the charge neutrality condition

$$Q_g + Q_o + Q_s = 0. \tag{2.3}$$

Under the assumption that the electric field is zero deep inside the bulk silicon and applying Gauss's law to the oxide silicon interface and gate oxide interface, the gate voltage can be rewritten as [21]:

$$V_g = V_{fb} + \phi_s - \frac{Q_s}{C_{ox}} = V_{fb} + \phi_s + \frac{\sqrt{2\varepsilon_{si} e N_b \phi_s}}{C_{ox}} \tag{2.4}$$

where V_{fb} is the flat band voltage, C_{ox} the oxide capacitance and ε_{si} the dielectric constant of Si. Equation (2.4) gives the relationship between the applied voltage and the surface potential. Depending on the value of V_g, one can distinguish between different surface conditions, i.e.

- $\phi_s < 0$ (accumulation): If the applied gate voltage V_g<V_{fb}, electrons are depleted from the interface (see Fig. 2.4(b)) leading to an excess accumulation of holes. As the hole concentration increases at the interface compared to that of the p-type bulk-Si, the bands bend upwards.

- $\phi_s = 0$ (flatband): This case is like the ideal energy-band diagram (see Fig. 2.2), the bands are flat.

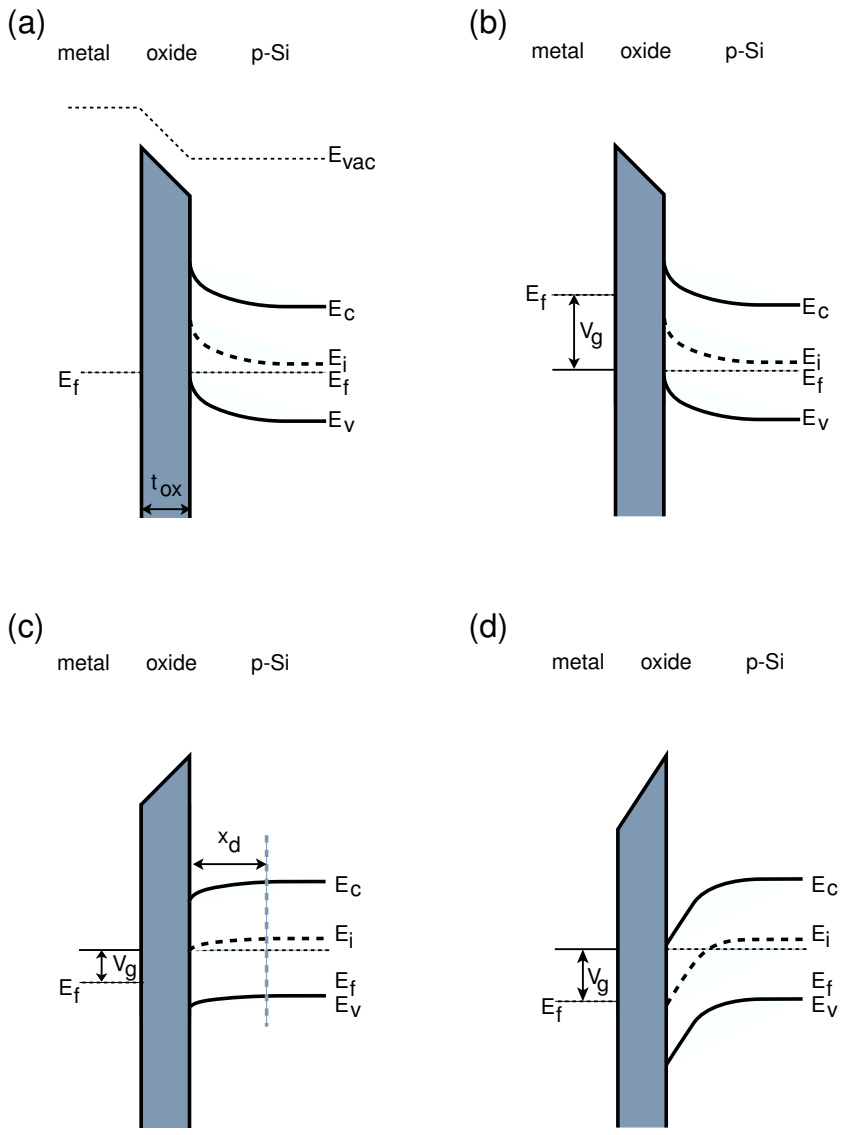


Figure 2.4: Effect of an applied voltage on a p-type MOS capacitor. (a) equilibrium, (b) accumulation, (c) onset of inversion, and (d) strong inversion.

• $\phi_b > \phi_s > 0$ (depletion): If the applied gate voltage $V_g > V_{fb}$, holes are depleted from the interface leading to a lower hole concentration compared to the p-type bulk-Si and hence the bands bend downwards (Fig. 2.2(c)).

• $\phi_s > \phi_b$ (inversion): If the applied gate voltage becomes sufficiently positive to attract a significant number of free electrons to the surface, the density of electrons will exceed the density of holes at the interface. This is called surface inversion because of the opposite situation expected in normal p-type Si (Fig. 2.2(d)).

• $\phi_s > 2\phi_b$ (strong inversion): With a further increase of gate voltage, the electron density at the interface finally begins to exceed the concentration of the acceptor atoms in the p-type Si. The surface potential ϕ_s remains constant because the inversion layer charge screens the gate induced electric field.

In case of n-type Si, the operating principle of the MOS capacitor is the same except that the inversion layer is made up of holes as minority carrier instead of electrons.

2.3 Schottky diodes

When a metal is in contact with a semiconductor, a Schottky barrier is formed at the interface. The potential barrier, i.e. the Schottky barrier, can be identified in the energy band diagram as shown in Fig. 2.5 for a Schottky diode on n-type silicon. Φ_m is the metal work function, i.e. the voltage necessary to remove an electron from the metal. χ is the electron affinity, i.e. the voltage necessary to remove an electron from the conduction band of the semiconductor. When the metal and the semiconductor are brought into contact, electrons leave the semiconductor with positive charge of the fixed ions staying behind, which creates an electric field in the negative direction. Electrons flow into the metal until the Fermi energy throughout the structure is constant. The SBH ϕ_{bn} is defined as the difference between the metal work function and semiconductor affinity. For a semiconductor, the sum of the barrier for electrons and holes equals the band gap E_g:

$$q(\phi_{bn} + \phi_{bp}) = E_g. \tag{2.5}$$

Note, that ϕ_{bn} is strongly influenced by the Fermi-level pinning effect, which is mainly caused by metal induced gap states (MIGS) or defects associated with

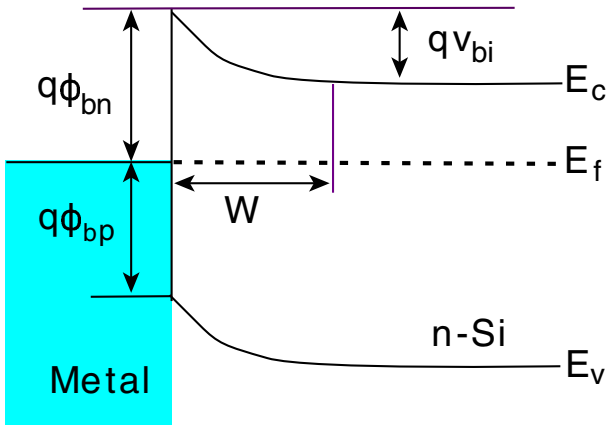


Figure 2.5: Schematic band-diagram of an ideal Schottky contact.

physical nonidealities of the interface such as dangling bonds [22]. In case of a large density of surface states on the semiconductor surface, electrons from the conduction band may be trapped in these surface states so that the impact of the metal on the semiconductor is screened. Hence, the SBH is not determined by the work function difference between the metal and the semiconductor but is determined primarily by the character of the metal and the interface property [23]. In order to avoid this effect, people have either used ultra-thin insulator film such as SiO_2 to block the metal induced gap states (MIGS) [24], while the SiO_2 is so thin that electrons can still tunnel through or they have used a passivation layer such as sulphur to remove the dangling bonds so that the real SBH will be determined by the difference of the work function [25]. Incorporation of a highly doped layer at the interface between the metal and the semiconductor or the whole bulk-silicon is highly doped, both ways can lead to a strong reduction of the effective SBH so that carriers can tunnel through the SB, but note that it does not change the real SBH.

Table 2.1 gives typical SBH of different metal silicides and most silicides have similar SBH because of the above mentioned Fermi-level pinning effect. The length W of the depletion region is similar to that in the $p-n$ junctions:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_{si}}{qN_b}(V_{bi} - V)}, \tag{2.6}$$

where ε_{si} is the dielectric constant of Si and V_{bi} is the built-in voltage. The length of the depletion region is dependent on the dopant concentration and the applied gate voltage. With increasing dopant concentration, W decreases. If the dopant concentration is larger than 10^{20}cm^{-3}, W is only on the order

Disilicides	ϕ_{bn}(eV)	Mono-silicides	ϕ_{bn}(eV)
$TiSi_2$	0.62	CoSi	0.68
$MoSi_2$	0.65	NiSi	0.64
WSi_2	0.65	IrSi	0.93
$NiSi_2$	0.66	PtSi	0.88
$TaSi_2$	0.59	MnSi	0.76
$ErSi_2$	0.39	RhSi	0.69

Table 2.1: Schottky barrier heights (ϕ_{bn}) of various silicides on n-type silicon.

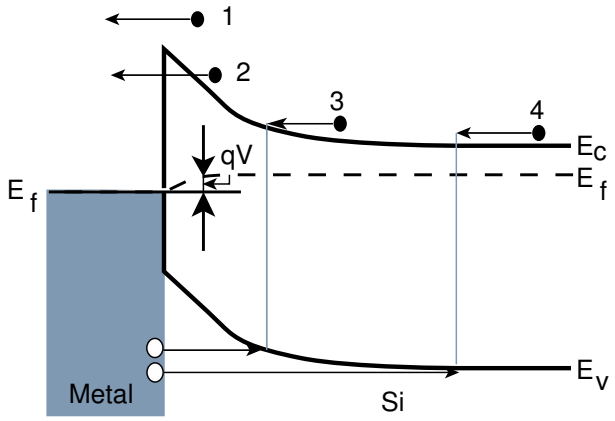


Figure 2.6: Four basic carrier transport mechanisms in a Schottky diode.

of a few nanometer.

2.4 Schottky diode current

Figure 2.6 shows a Schottky-diode under forward bias condition including the relevant carrier transport mechanisms which are:

1. Electrons overcome the Schottky barrier and travel from the semiconductor into the metal by thermal emission.

2. Electrons pass through the barrier by quantum-mechanical tunnelling.

3. Electrons and holes recombine in the space-charge region.

4. Holes are injected from the metal into the semiconductor.

The overall current can be approximately modelled by a combination of the thermal emission current and the tunnelling current for semiconductors with a high mobility and low density of defect states because in this case the current from electron-hole recombination (3) and hole injection (4) can be neglected. The first part of the electron transport over the potential barrier is the dominant process for Schotty diodes with moderately doped semiconductors (e.g., $\mathrm{N_b} < 10^{17}\mathrm{cm}^{-3}$). According to the thermionic theory of Bethe [26], only the carriers with energies larger than $q\phi_{bn}$ can overcome the Schottky barrier and contribute to the transport from the metal to the semiconductor or vice versa. Clearly, with increasing forward bias, the semiconductor remains at the same potential and the metal Fermi energy is shifted to lower energies due to the applied voltage and this in turn leads to a lowering of the barrier. Hence, current from the semiconductor to the metal (I^+) increases significantly. At the same time, the electron current from the metal to the semiconductor current (I^-) is very small because of a high and almost constant potential barrier between the metal and the semiconductor. Similarly, under reverse bias condition, I^+ is significantly decreased because the potential barrier is increased. Since the current I^- is almost voltage independent, therefore, the total current for forward and reverse bias can be very different. The sum of both current contributions is given by Eq. (2.7):

$$I = I_s \left(\exp\left(\frac{\mathrm{qV}}{\mathrm{nkT}} \right) - 1 \right) \tag{2.7}$$

with

$$I_s = AA^{**}T^2 \exp\left(\frac{q\phi_{bn}}{kT} \right), \tag{2.8}$$

where I_s is the saturation current, A is the diode area and the A^{**} is the effective Richardson-constant with $\frac{110\mathrm{A}}{\mathrm{cm}^2\mathrm{K}^2}$ for electrons and $\frac{40\mathrm{A}}{\mathrm{cm}^2\mathrm{K}^2}$ for holes. The ideality factor n is defined as

$$n = \frac{q}{kT} \frac{\partial V}{\partial(\ln(I))}. \tag{2.9}$$

This parameter describes all effects that lead to a deviation of the Schottky diode from an ideal diode (where $n = 1$). n is approximately independent of V and is usually larger than 1. There are many possible reasons for a non-ideal behavior of a Schottky-diode. The most common being a bias dependence of the SBH. Under certain conditions, it is possible for electrons with $E < q\phi_{bn}$ to penetrate the barrier by quantum-mechanical tunnelling

as is shown in Fig. 2.6. In case of a degenerately doped semiconductor, the conduction band bends strongly downwards to the Fermi-level and the depletion region W (see Fig. 2.5) becomes so thin that electrons have a substantial probability to tunnel through this barrier resulting in a lower effective SBH. The tunnelling current has the form

$$I_t \sim \exp(-q\phi_{bn}/E_{00}) \tag{2.10}$$

with

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_b}{\varepsilon_{si}m^*}}. \tag{2.11}$$

This equation indicates that the tunneling current will increase exponentially with $\sqrt{N_b}$.

2.5 Operating principles of SB-MOSFETs

The basic operating principles of a long-channel SB-MOSFET are illustrated in Fig. 2.7. A mid-gap, Fermi level pinning at the metal semiconductor interface is assumed as is appropriate for materials such as NiSi. The silicon channel is considered as being undoped for simplicity. Without external voltage, the energy band diagram is in equilibrium and is constant throughout the channel. Dependent on the gate voltage V_{gs}, the SB-MOSFET can either work as an n-type MOSFET (nMOS) or a p-type MOSFET (pMOS).

In case of the nMOS (Fig. 2.7(a)), the current flow is exponentially suppressed due to the large potential barrier at the source end. With increasing positive gate voltage, the conduction band is pushed down so that the SB width at the source contact is thin enough for electrons to tunnel through and traverse the channel region. The same arguments hold for the nMOS with negative V_{ds} as shown in Fig. 2.7(b).

In case of the pMOS (Fig. 2.7(c)), the valence band will be pushed up with increasing negative gate voltage so that the SB width at the drain contact becomes thin and increasingly transparent for holes. The same arguments apply for the pMOS with negative V_{ds} as shown in Fig. 2.7(d).

This ambipolar behavior, i.e. the possibility of operation as nMOS and pMOS of the same device, leads to a significant difference of the electrical performance if compared to conventional MOSFETs. This difference will be discussed in detail in the following sections.

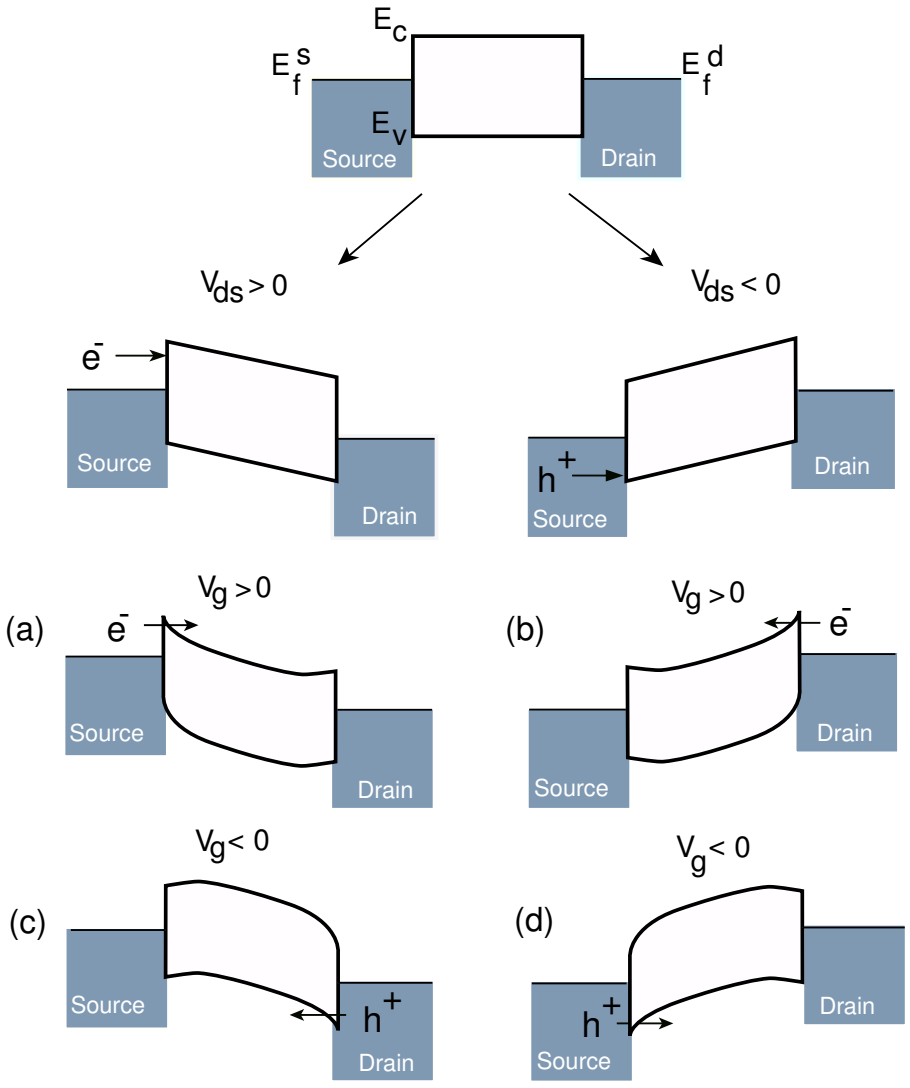


Figure 2.7: Schematic energy band diagrams to demonstrate the operating principle of SB-MOSFETs. (a)-(b) nMOS; (c)-(d) pMOS.

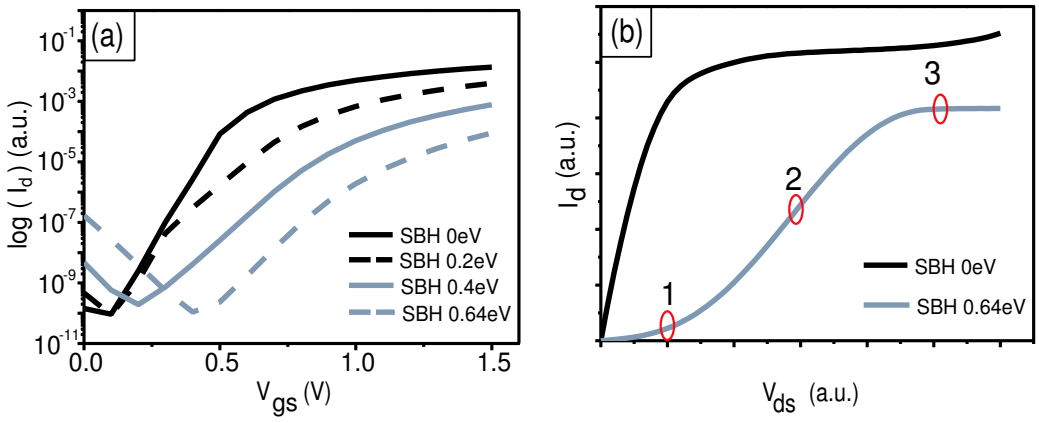


Figure 2.8: Transfer (a) and output (b) characteristics of a long-channel SB-MOSFET with different SBH. 1. Sub-linear region; 2. Linear region; 3. Saturation region.

2.6 I-V characteristics of SB-MOSFET devices

2.6.1 Long-channel SB-MOSFET

In this section we start with the discussion of the transfer and output characteristics of a typical SB-MOSFET, followed by the discussion of the figures of merit, namely the inverse subthreshold slope S and the transconductance g_m. Dependent on V_{gs} and V_{ds}, the operational region of SB-MOSFETs can be divided into subthreshold, sub-linear, linear and saturation regions.

Subthreshold region:
The subthreshold region usually characterizes the switching behavior of a transistor device. In this region the current is essentially an exponential function of the gate voltage. The required gate voltage needed to change I_d by one order of magnitude is called the inverse subthreshold slope S. In conventional MOSFETs with uniformly doped substrates S is given by

$$S = \ln 10 \left(\frac{\partial \log I_{ds}}{\partial V_{gs}} \right)^{-1} = 2.3 \left(\frac{kT}{q} \right) \left(1 + \frac{C_d}{C_{ox}} \right), \tag{2.12}$$

where C_d is the maximum depletion layer capacitance and C_{ox} is the gate oxide capacitance. Ideally, the inverse subthreshold slope is 60mV/dec at room temperature if $C_d \ll C_{ox}$. In case of SB-MOSFETs, however, the switching behavior is rather different due to the existence of the SB. Figure 2.8(a)

shows simulated transfer characteristics of SB-MOSFETs with different SBH. Obviously, as the SBH decreases from 0.64eV to 0eV, the device shows a significantly improved inverse subthreshold slope ranging from 120mV/dec to 60mV/dec, as well as a 100 times higher I_{on}/I_{off} ratio. As is well known, with the down-scaling of microelectronic devices, the supply voltage has to become smaller and smaller [1]. A large subthreshold slope as usually found in SB-MOSFETs with large barriers is therefore deleterious since it prohibits a further reduction of the supply voltage. Hence, SBH should be as low as possible in order to achieve reasonable I_{on}/I_{off} ratios. For logic applications, S must be less than 80mV/dec and the acceptable I_{on}/I_{off} ratios are in the range of $10^4 - 10^5$.

Sub-linear region:
The sub-linear region is a distinguished phenomena, typical of SB-MOSFETs. As is shown in Fig. 2.8(b), the S-shaped output characteristics (gray curve at very low drain voltage) is due to the formation of the SB at the drain, which prevents current flow until the drain bias is high enough [27]. When the SBH is smaller than $\sim 3kT$, this region will disappear and the device behaves like a conventional MOSFET (black curve).

Linear region:
The electron carriers injected from the Schottky contact into the channel region flow by satisfying the Poisson′s equation. In other words, the channel current can be described as the drift-diffusion current model using the current continuity condition between the tunneling and channel current. Therefore, this behavior can be illuminated by applying MOSFETs model [20]. In case of linear region, V_{ds} becomes larger and finally exceeds the SB at the drain side, the SB-MOSFET behaves like a resistor because the channel charge is kept constant and the change of drift velocity is proportional to the applied source-drain voltage. Clearly, in this region the drain current increases linearly with V_{ds} and can be approximated as [21]

$$I_d = \frac{\mu_{eff} C_{ox} W}{L}(V_{gs} - V_{th})V_{ds}, \tag{2.13}$$

where μ_{eff} is the effective electron mobility, V_{th} is the threshold voltage and W and L are the channel width and length.

Saturation region:
As V_{ds} increases further (for a given V_{gs}), the carrier density at the drain end decreases and the channel gets pinched off. The region $L - l_d$ is depleted and the pinch-off point of the channel moves toward the source with fur-

ther increased V_{ds} as shown in Fig. 2.9(b). The pinch-off region l_d between the pinch-off point and the drain end causes the effective channel length to decrease from L to $L - l_d$, which is referred as channel length modulation (CLM). The channel length of the long-channel SB-MOSFET can be regarded as constant for any V_{ds} in excess of the saturation voltage V_{dsat} (V_{ds} at the onset of pinch-off) due to $l_d \ll L$. The saturation current I_{dsat} can hence be written as

$$I_{dsat} = \frac{\mu_{eff} C_{ox} W}{2(L - l_d)} (V_{gs} - V_{th})^2. \tag{2.14}$$

In the saturation region, the ratio of the change of drain current to the

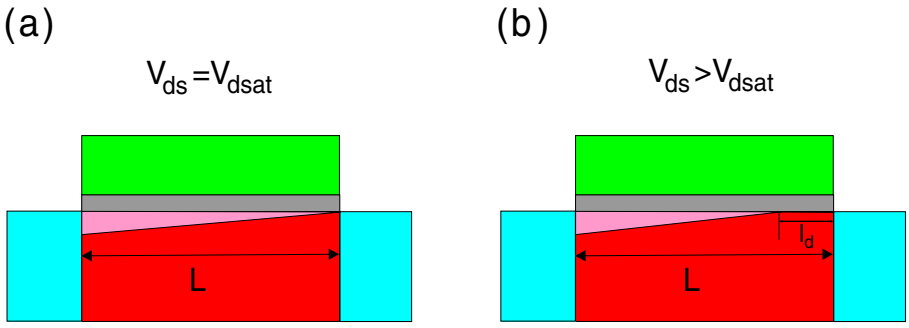


Figure 2.9: Schematic cross-section of a SB-MOSFET showing channel pinch-off as V_{ds} is increased (a) At the onset of saturation, the channel pinches off at the drain end and (b) the pinch-off point moves towards the source.

change of the gate voltage with constant V_{ds} is called gate transconductance g_m,

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{V_{ds}=const.} \sim \frac{1}{L \cdot t_{ox}} \tag{2.15}$$

which is normalized to the channel width of the transistor. A small channel length and a thin gate oxide results in a large g_m.

DIBL-like effect:

Figure 2.10 shows typical $I-V$ transfer characteristics of a SB-MOSFET under different source-drain biases. In the n-type operation region, an increasing V_{ds} leads to a large current change similar to drain induced barrier lowering (DIBL) in conventional MOSFETs. However, the origin of this DIBL-like effect is not a barrier lowering and is also observed in long channel SB-MOSFETs. The reason for its appearance can be seen when looking at the band-diagram as shown in Fig. 2.11(a): At a given gate voltage and

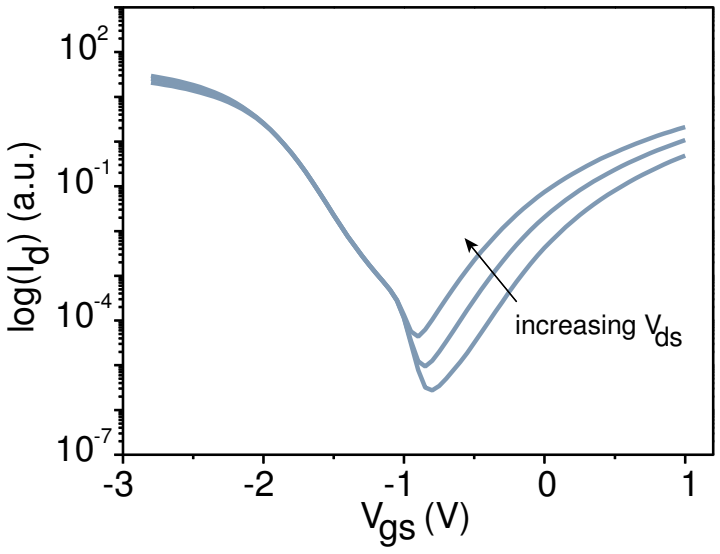


Figure 2.10: Transfer characteristics of SB-MOSFET with different negative V_{ds}.

negative V_{ds}, the on-currents mainly stem from the tunneling current of the electrons through the SB at the drain end. When V_{gs} is kept constant and V_{ds} becomes more negative, the SB width at the drain side becomes thinner as shown in Fig. 2.11(b) so that more electrons can tunnel through the SB into the channel. In such case increasing V_{ds} can also be regarded as increasing V_{gs} while V_{ds} is kept constant because both situations represent a relative Fermi-level shift. Therefore, increasing V_{ds} results in a large current change in the n-type operational region. This DIBL-like effect is not a short channel effect (SCE) but a typical behavior of SB-MOSFETs.

2.6.2 Short-channel SB-MOSFET

For short-channel devices, the potential distribution along the channel is strongly affected by source and drain, which modify the potential distribution of the entire channel: the depletion regions of drain penetrate deep into the channel region with increasing V_{ds} and influence the control of the channel charge by the gate. In this case a SB-MOSFET device exhibits a larger S and no saturation in the output characteristics. These phenomena are called SCE and deteriorate the device performance. Drain induced barrier thinning (DIBT) as mentioned in Ref. [16] is a typical SCE in SB-MOSFETs.

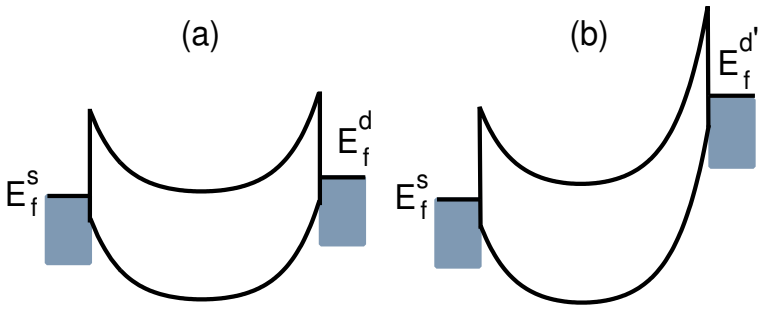


Figure 2.11: Energy band diagram of a SB-MOSFET with different negative V_{ds}. (a) small V_{ds} (b) large V_{ds}.

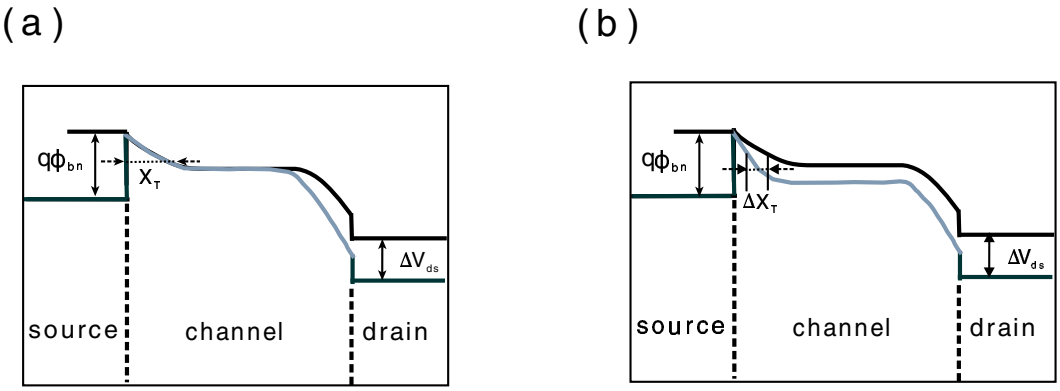


Figure 2.12: Schematic energy band diagram with different V_{ds} indicating the DIBT effect for (a) long-channel and (b) short-channel SB-MOSFETs .

In the on-state, when the drain voltage increases and a high electric field penetrates into the channel, the Schottky barrier width is thinned, leading to an increased tunnelling current. The comparison of the DIBT effect between long-channel and short channel devices is schematically shown in Fig. 2.12. For a long-channel device, the drain bias has little effect on the Schottky barrier width. However, in a short-channel device the Schottky barrier width is strongly affected by V_{ds}. In SB-MOSFETs, DIBT is defined as the ratio of change in threshold voltage (ΔV_{th}) to a change in drain voltage (ΔV_{ds}) in the subthreshold region with units of mV/V

$$DIBT = |\frac{\triangle V_{th}}{\triangle V_{ds}}|. \tag{2.16}$$

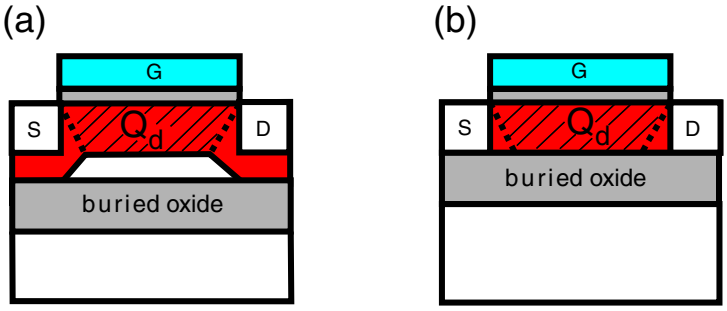


Figure 2.13: Partially depleted SOI MOSFET (a) versus fully depleted SOI MOSFET (b). Depicted is the depletion charge Q_d distribution which is controlled by the gate.

2.6.3 SB-MOSFESTs on bulk versus on SOI

With the down-scaling of conventional MOSFETs on bulk silicon SCE and a loss of electrostatic control by the gate deteriorate the device performance. Silicon on insulator (SOI) is an attractive material due to full isolation of the devices which substantially reduces most parasitic effects observed in bulk silicon devices. Additionally, because the dielectric constant of the buried insulator (usually SiO_2, called buried oxide (BOX)) is three times smaller than that of silicon, the parasitic capacitances between the source/drain junctions and the substrate are strongly reduced. This improves the response speed of such devices. The performance of SOI-MOSFETs is highly dependent on the thickness and the doping concentration of the silicon film [28]. There are two types of SOI transistors: fully depleted, in which the silicon film thickness t_{si} in the channel region is smaller than depletion depth at the threshold voltage and partially depleted, in which t_{si} is larger than depletion depth at the threshold voltage. For thick SOI films (>300 nm) on insulator, the devices approach the bulk limit.

Figure 2.13 shows the distribution of the depletion charges in a short channel device on partially and fully depleted SOI. Obviously, for partially and fully depleted devices, the gate controlled depletion charge, depicted by the trapezoidal hatched area under the gate, becomes smaller and smaller with decreasing channel length. However, the ratio of the trapezoidal hatched area to the whole depletion charge in the fully depleted SOI transistor is larger than in the partially depleted SOI transistor [28]. Therefore, partially depleted SOI devices suffer more from SCE than fully depleted SOI devices. Furthermore, the floating body in partially depleted devices can degrade the device performance because of an uncontrolled lowering of the

threshold voltage caused by a parasitic bipolar transistor action due to the charges generated by impact ionization at high source-drain voltages [28]. In a fully depleted device, the relative amount of depletion charge increases as the Si thickness decreases and thus the DIBL and roll-off of the threshold voltage is much smaller. In addition, fully depleted SOI devices eliminate all leakage paths because the potential barrier for any path between the source and drain is more strongly coupled to the gate than the drain and thus there is no need for channel doping. Furthermore, fully depleted SOI devices are immune to the floating body effect. The same argument can be applied for fully depleted SB-MOSFET devices. Ultra-thin body (UTB) SOI offers improved electrostatic gate control and enhanced device performance. If the SOI film thickness is reduced to 10nm or below quantum mechanical effects become important so that the energy bands split into subbands. As a result, the energy of the first subband rises, which increases the effective barrier height between source and drain. In addition, an enhancement of the electron effective mobility can be expected due to an increased occupancy of the 2-fold valleys for Si thickness t_{si} between 3nm and 5nm [29]. Below 3nm the mobility due to the roughness of the SOI film decreases [30]. From the analysis above, we can see that the use of UTB can reduce SCE and improve the device performance [31]. The Si thickness has to be chosen with care in order to find the optimum trade-off between the increase of the barrier height caused by band-splitting and the improved electrostatics with decreasing t_{si} in SB-MOSFETs. In Ref. [32], the best electrical performance was achieved for a device with t_{si} 4nm and 30nm channel length.

Chapter 3

Silicide in SB-MOSFET

A major problem for ultra-short channel devices is the increased series resistance in the source/drain region. Self-aligned silicidation (Salicide) is a well-known process to solve this problem. Figure 3.1 shows a typical salicide process for advanced CMOS. A metal film is deposited on a prefabricated gate structure with oxide or nitride spacers. During RTP annealing the metal reacts exclusively with Si or poly-Si regions and forms a silicide at source, drain and gate. The unreacted metal after silicidation can be selectively etched away. The spacer is very important for the electrical insulation between the gate and the source/drain in the fabrication.

Silicides are commonly used as ohmic contacts, Schottky contacts and interconnects. The advantages of silicides include a low parasitic resistance and a high thermal stability. $TiSi_2$, PtSi and $CoSi_2$ have been investigated as materials for salicide in the development of Si technology [33]. In case of $TiSi_2$, the transformation from the high resistivity phase (C49) to the phase with low resistivity (C54) is nucleation limited. Thus, for lines narrower than 0.35μm, the transformation becomes difficult and grains of the silicide become disconnected due to agglomeration [34, 35]. In order to suppress the narrow line effect additional processes such as pre-amorphization of silicon are needed [36]. $CoSi_2$ has also narrow lines effect. In addition, it builds up a higher stress during silicidation [37] and for the formation of $CoSi_2$ elevated temperatures are needed. Platinum silicide also causes problems if integrated into ICs because of its instability at high temperature cycles [38]. At the moment NiSi is the research favorite due to its low resistivity, low processing temperature, small silicon consumption and large processing window (400°C-700°C) [36]. Recent papers have shown that NiSi will become an indispensable material for the fabrication of nanoelectronic devices. Researches on NiSi concentrate on the formation of nickel mono-silicide phase and on its thermal stability. This chapter reviews the formation of nickel

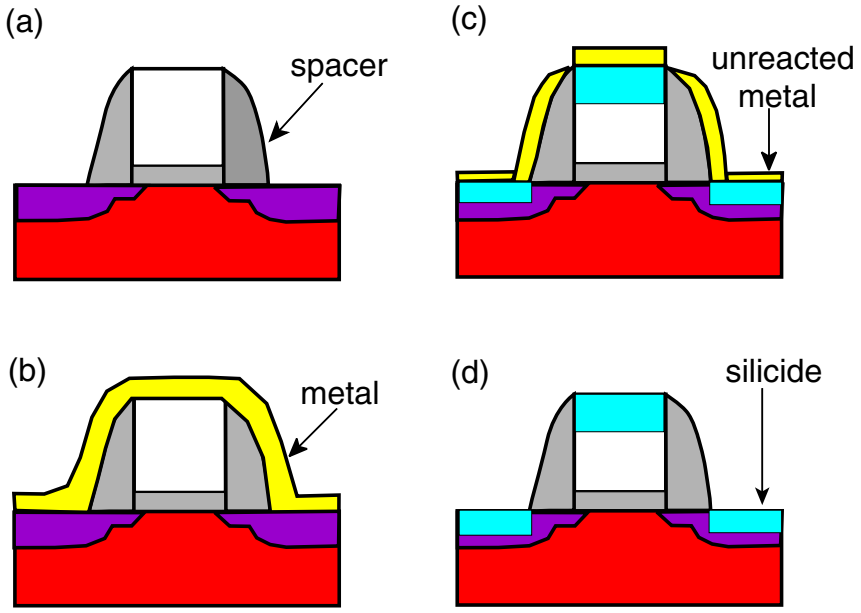


Figure 3.1: A typical salicide process. (a) MOSFET formation, (b) metal deposition, (c) silicidation by RTP annealing and (d) removal of unreacted metal.

silicide on Si-substrates and especially on SOI, followed by an investigation of the lateral growth of NiSi on thin SOI. Subsequently the silicide induced dopant segregation effect is studied in detail.

3.1 Silicidation of NiSi

Figure 3.2 shows the nickel-silicide phase diagram. There are three main stable phases Ni_2Si, NiSi, and $NiSi_2$ below 1000°C. Table 3.1 shows the main characteristics of these three phases. The crystal structure of silicon and NiSi is shown in Fig. 3.3. The single crystal of nickel silicide, NiSi, shows it to be orthorhombic with space group Pbnm and the unit cell contains four NiSi. $NiSi_2$ has a CaF_2 crystal structure with a lattice constant close to silicon and has the possibility of epitaxial growth.

The simplest way to form a thin silicide film is to deposit nickel on silicon and induce the silicide formation by rapid thermal annealing. Dependent on the annealing temperature, a metal rich phase forms first followed by mono-silicide and finally Si rich phase according to

$$Ni \rightarrow \alpha - Ni_2Si \rightarrow NiSi \rightarrow NiSi_2.$$

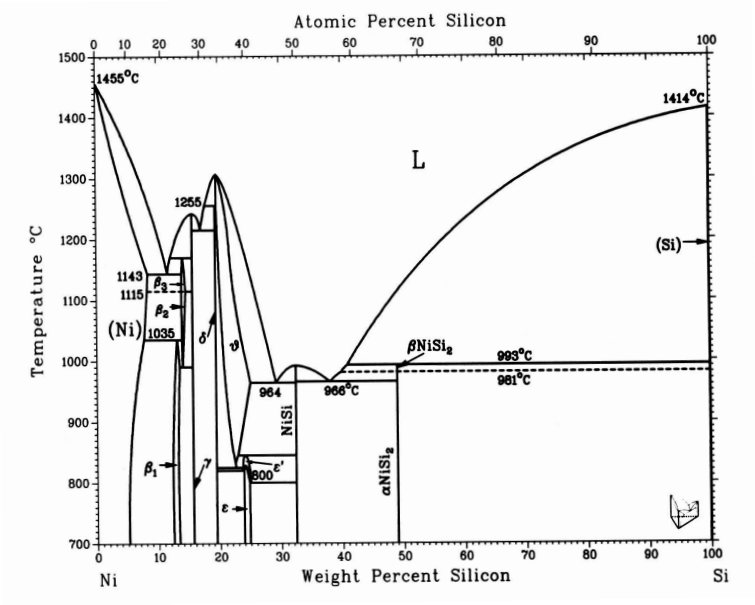


Figure 3.2: Nickel-Silicon phase diagram.

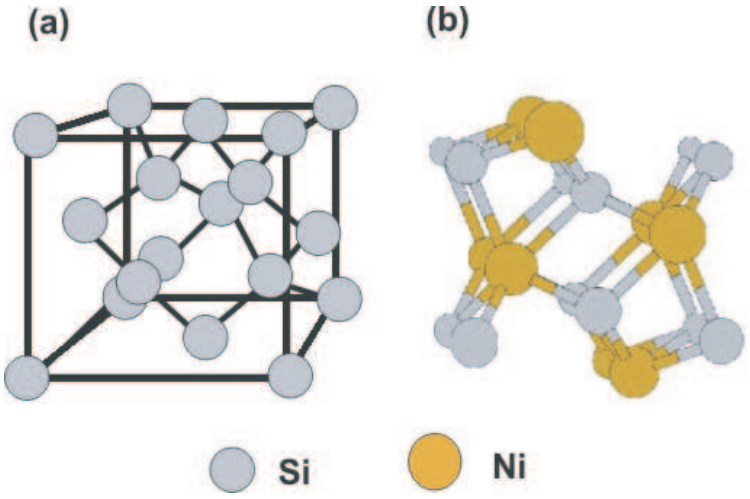


Figure 3.3: Crystal structure of (a) Silicon (Diamond structure) (b) NiSi (MnP structure)

Phase	Structure	Lattice constant($\dot{A}$)			T_m	T_f	ρ	ϕ_{bn}
		a	b	c	(K)	(^oC)	($\mu\Omega cm$)	(eV)
Ni_2Si	Orthorhombic	5.00	3.73	7.04	1580	200-325	24	0.66
NiSi	Orthorhombic	5.18	3.34	5.62	1265	350-600	10.5	0.65
$NiSi_2$	Cubic	5.40	5.40	5.40	1298	750-800	34	0.66

Table 3.1: Physical and thermochemical properties of the nickel silicides.

At about 250°C, the Ni film transforms into Ni_2Si. The growth is perpendicular to the Ni/Si interface until the total consumption of the Ni film. Upon increasing the temperature to about 300°C, Ni_2Si reacts with Si leading to NiSi. Above 450°C, NiSi becomes the dominant phase and $NiSi_2$ forms after RTP at T$\geq$ 650°C. Therefore, Ni_2Si, NiSi and $NiSi_2$ are the main silicide phases growing sequentially.

The growth of silicide films needs a continuous supply of silicon and Ni atoms at the interface. In case of NiSi, Ni is the dominant moving species which determines the growth rate due to its low activation energy for interstitial diffusion in Si. In addition, it softens the Si covalent bond strength to generate a flux of Si atoms forming a silicide at low temperatures [39]. For the formation of nickel mono-silicide one normally uses a one-step or a two-step rapid thermal annealing process [11, 40]. A two-step process is often employed to obtain a complete conversion to the preferred Ni monosilicide phase when fabricating shallow junctions of source and drain contacts in conventional MOSFETs without lateral silicide growth.

3.1.1 NiSi films on Si(100)

We start with p-type doped Si substrates with a resistivity of $2000\Omega cm$. In order to characterize the Ni/Si reaction, 40 nm Ni is deposited by electron-beam (E-beam) evaporation in high vacuum ($\sim 10^{-7}$ Torr). After Ni deposition, the sample were annealed at different temperatures that correspond to the phase formation windows for Ni_2Si, NiSi and $NiSi_2$. The same process was repeated with samples implanted with 5 keV As^+ ions and a dose of $10^{15}cm^{-2}$. Figure 3.4 shows the sheet resistance of nickel silicide film on both substrates, which is in good agreement with results reported in Ref. [41]. At 350°C, the layer is a mixture of Ni_2Si and NiSi. From 450°C to 800°C, NiSi is the dominant phase with a constant sheet resistance. When NiSi is transformed into $NiSi_2$ at higher temperatures, the silicide thickness and the sheet resistance increase because $NiSi_2$ has a two times higher sheet resistivity compared to NiSi. In the range from 350°C to 450°C the sheet re-

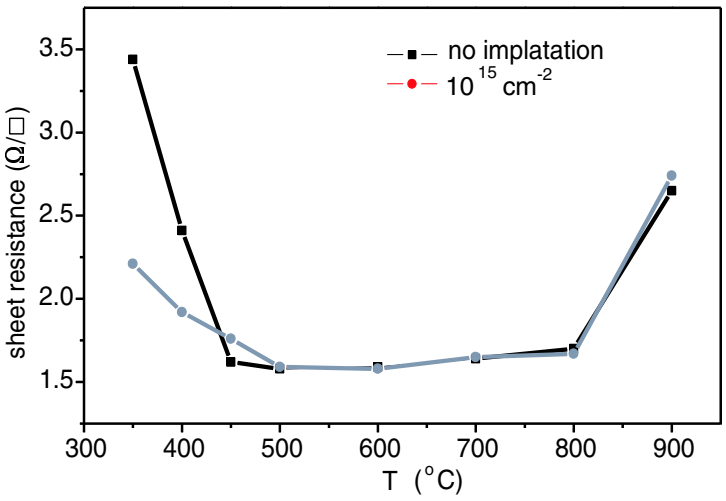


Figure 3.4: Sheet resistance versus annealing temperature. All samples were annealed for 30s.

sistance continues to decrease because NiSi becomes dominant in the silicide film. Then, the sheet resistance remains constant over a large temperature window, i.e. from 450°C to 800°C, which indicates that NiSi is the dominant phase and rather stable. Results of Rutherford backscattering spectroscopy (RBS) have confirmed the expected thickness of the NiSi layer with a specific resistivity of about 12$\mu\Omega$cm. For annealing temperatures over 800°C, sheet resistance increases significantly. The formation of a multi-phase at 350°C and 800°C is confirmed by the ratio of Ni and Si in the RBS spectra in Fig. 3.5. In case of highly-doped substrates, the resistivity in the range from 450°C to 500°C is higher than in case of a lowly-doped substrate due to the dopant retarded silicidation [42]. A temperature of 500°C is thought to be the most appropriate annealing temperature to form high quality NiSi on bulk-Si. According to Ref. [43, 44], a silicon-rich phase $NiSi_2$ may form at lower temperatures for thin films ($\leq$22nm NiSi) or in small-dimension contact holes.

3.1.2 NiSi films on SOI(100)

Since there has been considerable interest in fabricating devices on SOI, we investigate the formation of NiSi on SOI. Source/drain engineering on SOI is rather different from bulk-Si because of the limited silicon thickness. For UTB SOI the exact thickness of the deposited nickel layer is required to

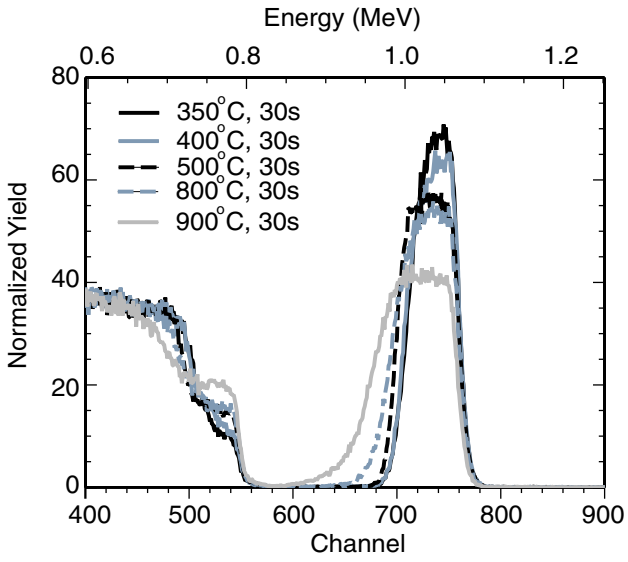


Figure 3.5: RBS spectra of nickel silicide film on silicon substrate at different annealing temperatures.

realize a mono-silicide phase ($1\text{nm}\,\text{Ni} + 1.84\text{nm}\,\text{Si} \rightarrow 2.22\text{nm}\,\text{NiSi}, 1\text{nm}\,\text{Ni} + 0.91\text{nm}\,\text{Si} \rightarrow 1.4\text{nm}\,\text{Ni}_2\text{Si}$) [43].

For the formation of fully silicide NiSi films on 50 and 10nm SOI, 30nm and 6nm Ni were deposited. To ensure a full silicidation, the thicker layer was annealed at 500°C for 30s and thin ones at 400°C for 18s. Figure 3.6(a) shows the RBS spectra of a silicide layer formed with a one-step annealing procedure on 50nm SOI. The sheet resistance is $2.7\Omega/\square$ resulting in a specific resistivity of $16\mu\Omega\text{cm}$, which is higher than the resistivity value of $12\mu\Omega\text{cm}$ on a control bulk-Si sample annealed under the same conditions. The larger sheet resistivity observed after a one-step annealing silicidation for the SOI samples stems from the formation of a metal-rich phase as indicated by the RBS spectra. In case of the 10nm SOI, the specific resistivity increases to $20\mu\Omega\text{cm}$. The RBS spectra (Fig. 3.6(b)) shows a higher Si signal suggesting $NiSi_2$ silicon rich phase, which is formed at much lower temperature on thin silicide film than on the thick silicide film.

Figure 3.7 shows TEM images of fully silicided layers on different SOI films. The existence of a silicide layer consisting of different phases in both cases ((a) and (b)) is indicated by the different contrast of the silicide grains. The chosen Ni thickness leads to an excess of Ni for the monosilicide formation which is not desirable. However, in order to get a good Schottky contact (see Fig. 7.10(a)) directly under the gate in a SOI SB-MOSFET device, we

have to deposit more Ni than necessary because ultra-thin gate spacers can not be formed in the present processing technology. Concerning the thickness of Ni deposition, it will be discussed in the section 3.3.

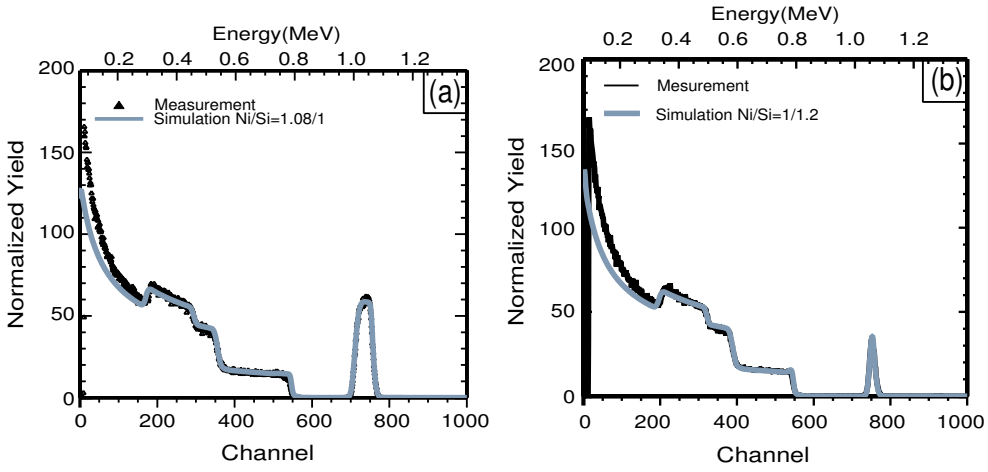


Figure 3.6: RBS spectra of nickel silicide layers formed on (a) 50nm SOI (b) 10nm SOI.

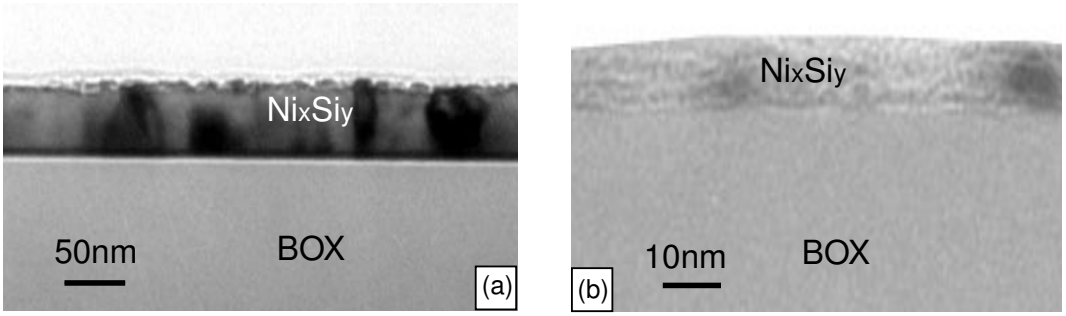


Figure 3.7: TEM image of a fully silicided layer on (a) 50nm SOI and (b) 10nm SOI.

3.2 Silicidation induced dopant segregation

If the silicidation is carried out in doped samples, dopants are found to redistribute between the silicide and the silicon which affects the electrical

properties of Schottky contact [45, 46]. Whether dopant redistribution occurs or not is determined by the diffusivity and solid solubility of the dopants in the silicide and the presence of point defects at the silicide-silicon interface. Thermal annealing of Ni on ion implanted silicon can induce dopants to redistribute during the silicidation. In particular, dopants segregate at the interface because of the different solubilities in both materials. In case of the NiSi phase, nickel atoms are the moving species, supplied by the diffusion through the growing silicide layer to the silicide/Si interface, because the covalent bonds between Si atoms are softened by diffusing Ni atoms [39]. A significant change of volume is involved when the silicide is formed, which leads to a high strain at the interface. As a result, point defects (self -interstitial or vacancies) can be generated in order to partially relieve the stress. Due to the formation of vacancies, the diffusivity of arsenic in silicon is enhanced and arsenic is pushed out of the silicon after silicide is formed at the former location of the silicon and moves towards the interface where it piles up at the moving interface between silicide and silicon [39]. Although the dopant concentrations are generally below the solid solubility limit in silicides and silicon, the high strain interface induced point defects can lead to local dopant concentration higher than the solid solubility [39]. In Ref. [47], silicidation induced dopant segregation is found to take place at the interface between the silicide and the gate oxide, which is used to adjust work function of the gate electrode.

In order to confirm the segregation of dopants at the NiSi/Si interface and quantify the dopant concentration, ToF-SIMS (secondary ion mass spectrometry) was used to analyze the depth distribution profiles of dopants in test samples. In case of As segregation, samples are prepared by arsenic ion implantation at 5 keV with different doses into bulk silicon. Directly after a diluted HF dip (DHF), nickel is deposited followed by a thermal annealing at 500°C for 90s. The composition of the silicided film was controlled by RBS and four point measurements. The resulting SIMS depth profiles are shown in Fig. 3.8(a) for three different arsenic implantation doses. There are three As peaks in the SIMS profile. The first one corresponds to the initial implantation peak and the second one may be due to the formation of different nickel silicide phases (like Ni_3Si_2). The pronounced peak at a depth of ∼100 nm corresponds to the silicide-silicon interface and indicates that the entire doped area is silicided. In case of B segregation, samples are prepared by boron ion implantation at 2 keV with different doses, followed by the same heat treatment as the As samples. The B segregation (see Fig. 3.8(b)) also occurs at the interface between the silicide and the silicon due to the lower solubility of boron in the silicide as compared to silicon. No other peaks of boron in the silicide film and a much larger out diffusion length into the Si

are observed, which may be attributed to the higher diffusivity of boron in both materials.

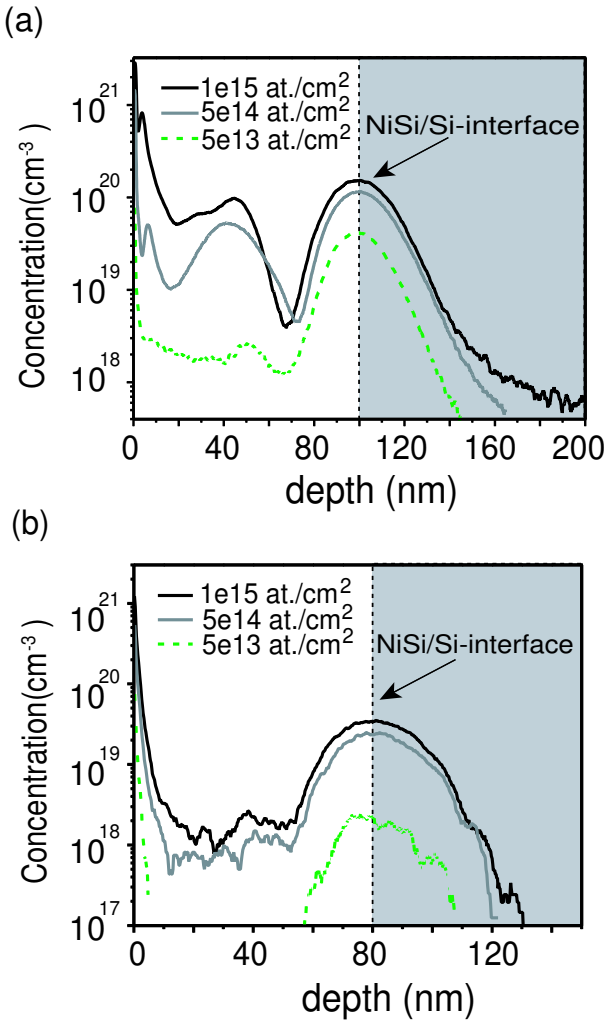


Figure 3.8: (a) As segregation at the NiSi/Si interface and (b) B segregation at the NiSi/Si interface. Three different implantation doses were investigated.

3.3 Lateral silicidation of NiSi on SOI

When working with fully silicided source/drain contacts, the lateral diffusion of NiSi during silicidation may cause severe encroachment of NiSi into the channel. When the silicide consumes the entire highly doped region of a

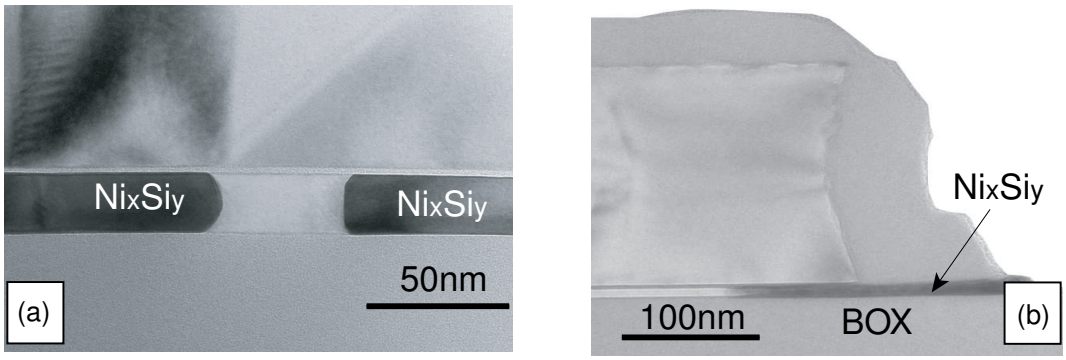


Figure 3.9: XTEM micrograph showing (a) aggressive lateral growth of Ni_xSi_y under a 1 μm gate length. The spacing between the Ni_xSi_y contacts shrank to 50nm during silicidation at 500°C for 1min. (b) Well controlled Ni_xSi_y encroachment at 400°C for 18s for a 1 μm channel length.

conventional MOSFET, the device will eventually become a SB-MOSFET device. On the other hand, since SB-MOSFETs need silicide-silicon interface

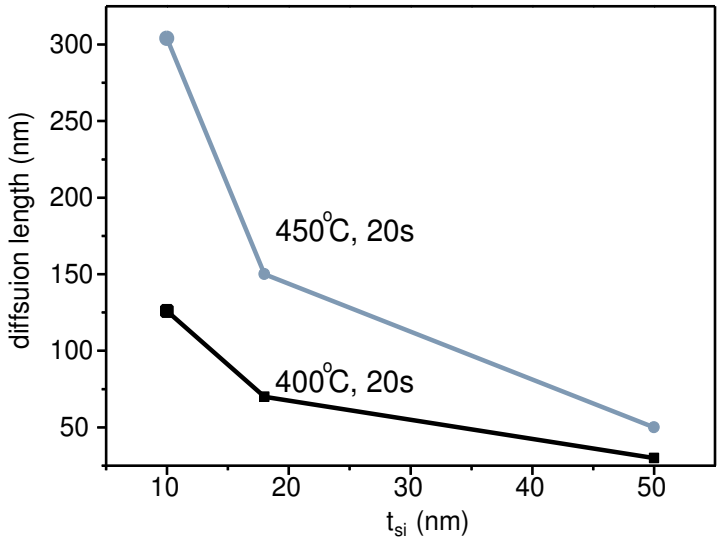


Figure 3.10: Lateral Ni_xSi_y growth under the gate spacer and into the channel versus SOI thickness for two annealing conditions.

right at or somewhat into the channel region, the above mentioned problem is not an issue for the SB-MOSFETs in our present study because it is only

related to the DC characteristics of SB-MOSFET. However, for ultra-short channel transistors, aggressive lateral growth can make device either with large leakage currents or short the transistor when the whole channel region is fully silicided [48].

Therefore, an excellent control of the silicidation reaction is indispensable for the realization of short-channel device. In addition, if we want lateral dopant segregation to take place in the SB-MOSFET (see section 7.1.4), a locally high dopant concentration is required. Therefore, the location of the silicide-silicon interface is very critical. A large lateral NiSi growth reduces the dopant concentration at the silicide/Si interface. If a one step annealing is used, the lateral growth depends sensitively on the SOI thickness, the annealing time and temperature. Figure 3.10 shows the lateral movement of the silicide front as a function of the SOI thickness for 20s anneals at 400°C and 450°C, respectively. The diagram shows clearly that the NiSi encroachment becomes very large at Si thicknesses below 20nm and high temperature anneals. In order to control the lateral growth, we either have to control the Ni layer thickness precisely or use an appropriate thermal treatment which allows a Si:Ni ratio $\geq$1.84. In our present experiments, we use an optimized thermal budget to control the encroachment of nickel silicide into the channel region.

Chapter 4

Modelling of SB-MOSFET operation

Simulations of single-gated short-channel fully depleted SOI SB-MOSFETs will be presented in this section in order to investigate the impact of the SOI thickness t_{si} and the gate oxide thickness t_{ox} on the electrical performance of SB-MOSFET devices. In addition, the impact of silicidation induced dopant segregation will be investigated. Instead of classical calculations, we use a quasi one-dimensional model based on a self-consistent solution of the Poisson and the Schrödinger equations as appropriate for ultra-small MOSFETs [32].

4.1 Model of device simulation

The model used here is based on a single-gated fully depleted SOI MOSFET with an undoped channel which is connected to source and drain contacts. Equation (4.1) is the two-dimensional Poisson equation,

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial z^2})\Phi(x,z) = \frac{\rho(x,z)}{\varepsilon_{si}}, \tag{4.1}$$

where $\Phi(x,z)$ represents the electrostatic potential and $\rho(x,z)$ is the charge density. In order to make the calculation efficient, the potential distribution vertical to the channel is approximated by a parabolic equation, so that the two-dimensional potential distribution is reduced to a one-dimension one along the channel [49]. After inserting the appropriate boundary conditions with the assumed parabolic equation, the following one-dimensional modified Poisson equation for the surface potential $\Phi_f(x)$ is obtained:

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\Phi_f(x) - \Phi_g + \Phi_{bi}}{\lambda^2} = \frac{\rho_{tot}(x)}{\varepsilon_{si}} \quad \text{with} \quad \lambda = \sqrt{\frac{\varepsilon_{\mathrm{si}}}{\varepsilon_{\mathrm{ox}}} \mathrm{t_{si}} \mathrm{t_{ox}}}, \tag{4.2}$$

where Φ_g and Φ_{bi} are the applied gate potential and the built-in potential. The screening length λ in the one-dimensional reduced Poisson equation is the relevant length scale on which potential variations are being screened. It sensitively depends on the channel and gate oxide thicknesses. Quantum simulations are performed by solving the Schrödinger equation with the non-equilibrium Green's function (NEGF) formalism [50]. The current is then calculated using the Landauer-Buttiker formula when self-consistency between the transport equation and the Poisson's equation is achieved. Additionally, quantum confinement in vertical direction is taken into account. Gate leakage is not included for simplicity in this model. Note, that in order to ensure the validity of the one dimensional model chosen here, the channel thickness t_{si} should be much smaller than depletion length [32]. In chapter 7, this model will be compared with experimental data and its range of validity will be further examined.

4.2 Simulation results

In the following sections, simulations are performed employing the modified one-dimensional model to investigate the electrical behavior of single gated, short channel, fully depleted SOI SB-MOSFETs. Ballistic transport is assumed in all simulations. This allows to give an upper estimate of the possible device performance. All simulations were performed for room temperature and a gate width of 4μm.

4.2.1 A 30nm device

Figure 4.1(a) shows transfer characteristics of a 30nm device with a SBH of 0.64eV and t_{ox}=2nm and t_{si}=10nm. V_{ds} and V_{gs} are as indicated in the figure. The $I-V$ transfer characteristics show a typical ambipolar behavior. The selected geometrical parameters yield the effective screening length to be $\sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{si} t_{ox}}$=7.8nm and the device shows clear short channel effects. A closer inspection shows a drain induced barrier thinning (DIBT) of 66mV/V, which means the effective screening length is still too large and the depletion charge in the channel is strongly influenced by the drain contact. Figure 4.1(b) shows the corresponding conduction band diagram in the channel. The minimal potential in the channel is not constant in the on-state for ballistic transport and changes with source-drain voltage. This is a clear evidence that the device suffers from SCE. The extracted inverse subthreshold slope of 173mV/dec is far away from the ideal case. However, as discussed in chapter 2, the bad switching behavior of this device is mainly due to the high SBH rather than

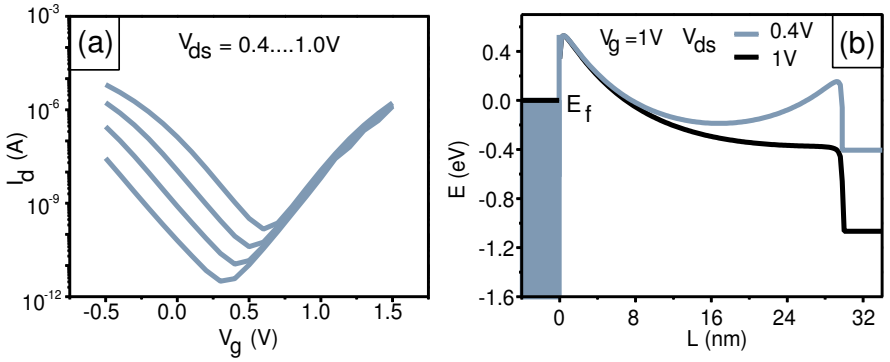


Figure 4.1: (a) Simulated transfer characteristics of a 30 nm SB-MOSFET with a SBH of 0.64eV, t_{ox}=2nm, t_{si}=10nm. (b) Energy band diagram in the channel for different source-drain voltages.

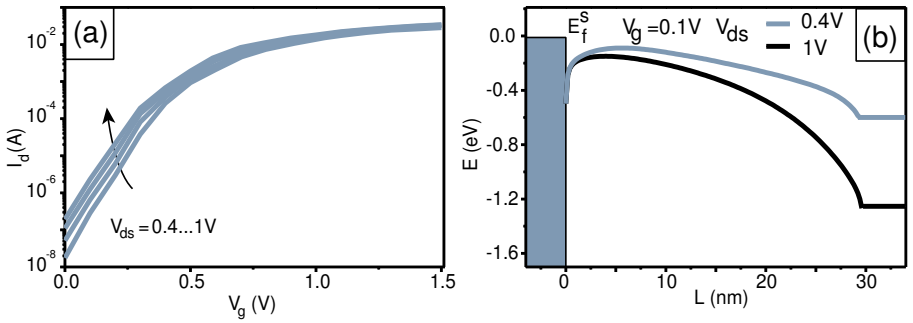


Figure 4.2: (a) Simulated transfer characteristics of a 30 nm SB-MOSFET with a SBH of -0.2eV, t_{ox}=2nm, t_{si}=10nm. (b) Energy band diagram in the channel for different source-drain voltage.

the present DIBT effect.

The simulations are also performed for a device with the same geometrical parameters but with a negative SBH because a negative barrier is needed in order to get a performance similar to a conventional MOSFET [51]. Figure 4.2 shows a clear increase of SCE if compared to a SB-MOSFET with a SBH of 0.64eV. Some authors have concluded that SB-MOSFETs exhibit less SCE than conventional MOSFETs [52]. This effect can be attributed to the reduced electric field near the drain because the Schottky barrier produces a built-in field with opposite direction to the applied source drain voltage [53]. Therefore, at a given V_{ds} the influence of the drain on the channel is lowered for SB-MOSFETs. However, it must be noted that the comparison of SCE in

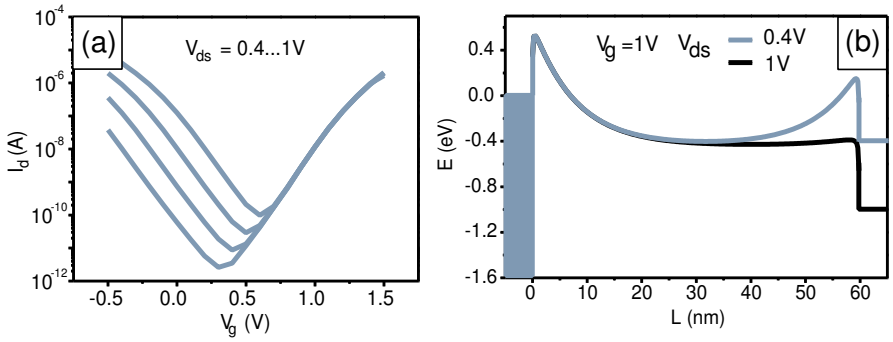


Figure 4.3: (a) Simulated transfer characteristics for a 60 nm SB-MOSFET with a SBH of 0.64eV, t_{ox}=2nm, t_{si}=10nm. (b) Energy band diagram in the channel for different source-drain voltages.

this way is meaningless since the current of both devices is not at the same level.

A heavily doped channel can suppress SCE but results in a degraded carrier mobility and enhanced junction leakage. An attractive way to suppress SCE without using heavily doped channels is the incorporation of ultra-thin gate oxides and ultra-thin SOI films [54]. The simulations are firstly performed for a device with a channel length of L=60nm to investigate the channel length dependence as is shown in Fig. 4.3. The potential profile in the channel does not change at different V_{ds}. If the channel length increases such that SCE disappear, the current should be constant for different channel lengths because the model used here only takes ballistic transport into account. Next, we use a thinner silicon film and gate oxide than that of the device in Fig. 4.1(a). As displayed in Fig. 4.4(b), the difference of the minimal potential in the conduction bands for different V_{ds} becomes less if compared to the energy band diagram in Fig. 4.1(b). This is a clear signature of suppressed SCE by thinning the SOI. Additionally, the difference of the minimal potential in the conduction bands for different V_{ds} disappears when the gate oxide is further decreased down to 1nm as is shown in Fig. 4.4(d). Comparing all the figures above we can observe that a reduction of the screening length λ results in reduced SCE and a better gate control over the channel. If the screening length λ is smaller than $L/6$, the device does not exhibit SCE.

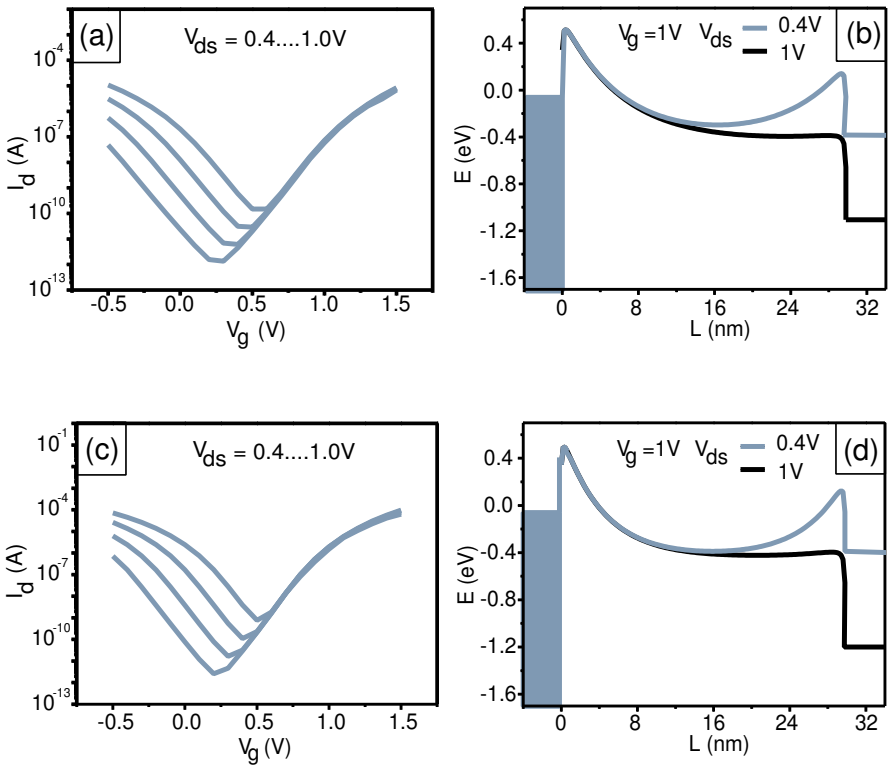


Figure 4.4: (a) Transfer characteristics of a 30 nm SB-MOSFET at different V_{ds} with a SBH of 0.64eV, t_{ox}=2nm, t_{si}=6nm. (b) Barrier lowering becomes less as compared to Fig. 4.1. (c) t_{ox}=1nm, t_{si}=6nm. (d) The minimum potential in the conduction band no longer depends on V_{ds}.

4.2.2 Gate oxide thickness

Since SCE can be avoided under the conditions stated above, the questions arise how the gate oxide thickness influences the electrical behavior of the devices apart from merely reducing SCE. The performance metric for intrinsic gate delay is $C_g V_{dd}/I_d$, where C_g is gate capacitance and I_d is the drive current. For conventional MOSFETs, t_{ox} should be as large as tolerable still avoiding SCE. Because I_d is proportional to C_g, the intrinsic gate delay does not depend on the gate capacitance and hence the actual gate oxide thickness is irrelevant. A thick gate oxide is preferable because it suppresses gate leakage. In case of SB-MOSFETs on the other hand, I_d is strongly dependent on $\sqrt{t_{ox}}$ in the subthreshold region, if the SB is approximated by a triangular potential well and a WKB approximation is used to determine

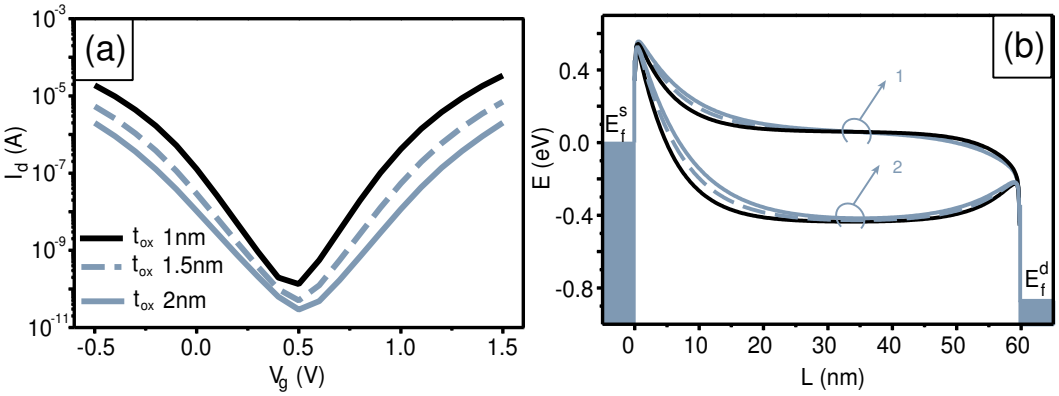


Figure 4.5: (a) Transfer characteristics for a 60 nm SB-MOSFET at V_{ds} 0.8V with SBH 0.64eV, t_{si}=10nm but different t_{ox}. (b) Energy band diagram for off-state (1) and on-state (2).

the tunneling current through the barrier. Therefore, I_d is much more sensitive to a change of the gate oxide thickness if compared to conventional MOSFETs. Obviously, the smallest intrinsic delay can be achieved in SB-MOSFETs with the thinnest gate oxide as long as gate leakage is sufficiently small. This behavior is clearly different from conventional MOSFETs. The detailed investigation of the impact of the gate oxide thickness t_{ox} on the $I-V$ characteristics is shown in Fig. 4.5. The SB-MOSFET with t_{ox}=2nm has a subthreshold swing of S=162mV/dec and S becomes smaller with decreasing gate oxide thickness. For the device with t_{ox}=1.5nm one gets S=150mV/dec and for t_{ox}=1nm, S=134mV/dec. An improvement is also observed in the on/off ratio. A closer look at the energy band diagram for the off-state denoted as 1 in Fig. 4.5(b) shows that the SB width at the source contact is the smallest for the t_{ox}=1nm device, which promotes a higher tunneling probability in comparison with other devices with thicker gate oxides and ensures improved switching behavior. The constant potential in the channel with varying V_{ds} means that all devices are long-channel transistors. In case of the on-state denoted with 2 in Fig. 4.5(b), the potential in the channel is rather different. This is not a SCE but an effect arising from the different ability of charge control by the gate. This implies that the thinner the gate oxide, the better the gate control and the thinner the Schottky barrier width. Therefore, the tight gate control is always desirable because of reduced SCE as well as an increased on-current. In order to investigate the impact of the gate oxide thickness on devices with various SOI thicknesses, simulations are also performed for devices with 2nm and 10nm gate oxide

and SOI thickness of 6nm and 12nm. For a device with 2nm gate oxide, S changes from 146mV/dec to 182mV/dec i.e. a variation of 28%, when SOI thickness increases from 6nm up to 12nm. For a device with 10nm gate oxide, S changes from 260mV/dec to 358mV/dec yielding a 38% variation for SOI thicknesses from 6nm to 12nm. Hence, although the variation of SOI thickness is the same, the variation of S is rather different. The simulation results demonstrate how important it is to work with ultra-thin gate oxides in order to lower the impact of SOI thickness variation and to ensure the functionality of an integrated circuit consisting of millions of transistors.

4.2.3 Silicon body thickness

Figure 4.6(a) shows transfer characteristics of devices with t_{ox}=1nm but different t_{si}. Devices with t_{si}=8nm have an inverse subthreshold slope of 122mV/dec. For t_{si}=6nm, S is equal to 112mV/dec and for t_{si}=4nm, S is equal to 94mV/dec. Clearly, with the decrease of the channel thickness, the electrical performance is strongly improved. In addition, the device with 4nm channel thickness has the lowest off-current and the highest on-current compared to the other two devices. It is important to note that due to quantum confinement effect, the t_{si}=4nm device has a larger effective SBH than the other devices. However, owing to the better gate control, the t_{si}=4nm device shows an increased tunneling probability although the barrier is slightly higher due to quantum confinement as shown in Fig. 4.6(b). This is reflected by a much larger on-current. The bulk potential in the channel in the on/off states remains constant for all three Si thicknesses, which is different from the case in Fig. 4.5(b). This difference indicates that the impact of the same relative percent change in the channel thickness and in the gate oxide thickness on the electrostatics of the devices is rather different and the scaling of the gate oxide is more important than the channel thickness. A summary of these results will be give in section 4.3.

4.2.4 Dopant segregation

As demonstrated in chapter 3 during silicidation induced dopant segregation, a highly doped layer can be formed at the silicide-silicon interface which may be used to modulate the effective SBH. In the following simulations, the impact of dopant segregation on the electrical performance of the devices will be investigated. All devices have t_{ox}=1nm, t_{si}=6nm and L=60nm if not stated otherwise.

The effect of dopant segregation is incorporated by a step function like doping profile with a spatial extension l_{seg} and a dopant concentration N_{seg}

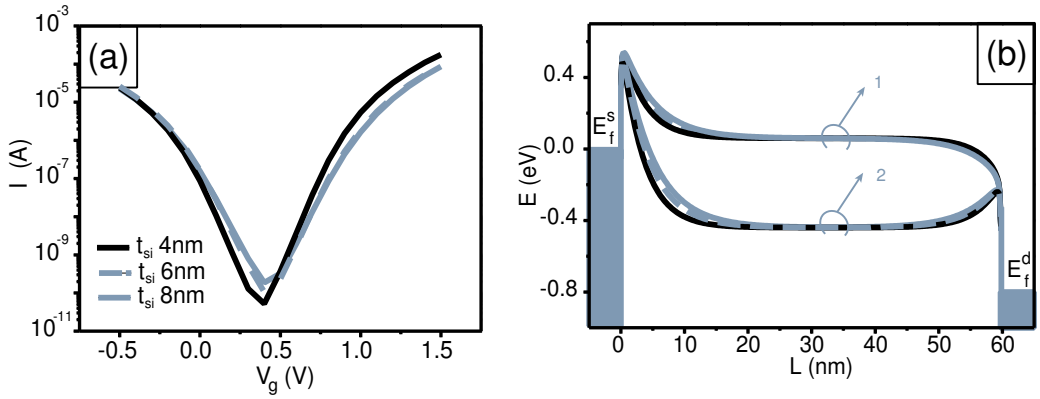


Figure 4.6: (a) Transfer characteristics for a 60 nm SB-MOSFET at V_{ds} of 0.8V with a SBH of 0.64eV, t_{ox}=1nm but different t_{si}. (b) Energy band diagram for off-state (1) and on-state (2).

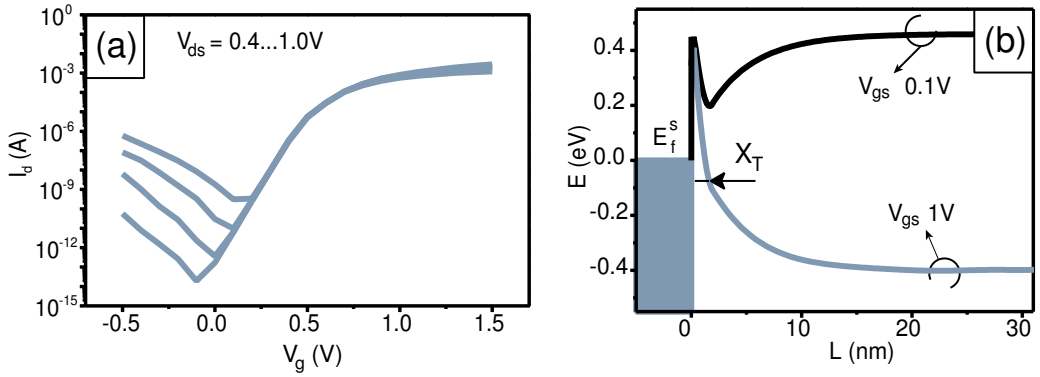


Figure 4.7: (a) Transfer characteristics of SB-MOSFET with dopant segregation. (b) Energy band diagram at two different gate voltages for a device with dopant segregation. l_{seg} =2nm, N_{seg}=2×10^{20}cm^{-3} and V_{ds}=0.8V.

right at the silicide-silicon interface. It is important to note that, if the whole channel region is highly doped, the transfer characteristics of a fully depleted device should be the same exhibiting only a threshold voltage shift. Therefore, a non-uniform doping profile is necessary as can be realized with dopant segregation. Simulation results show that the device performance is rather dependent on the dopant concentration as well as on the segregation length of the segregation region.

Figure 4.7(a) shows transfer characteristics of simulated devices with dopant segregation at different V_{ds}. Figure 4.7(b) displays the conduction and the valence band for a SB-MOSFET with dopant segregation at different gate voltages. As mentioned above, the highly doped region at the interface bends the conduction band strongly downwards to the Fermi-level (for n-type doping). As a consequence, the Schottky barrier width becomes so thin that the SB becomes highly transparent for electrons. Thus, the current flow at V_{gs}=0.1V (corresponding to the off-state) is determined by the bulk potential inside the channel instead of the SB at the source contact. Therefore, the current is determined by thermal emission in the off-state as in conventional MOSFETs and the inverse subthreshold slope is equal to the thermal limit 60mV/dec (Fig. 4.7(a)). This demonstrates a significant improvement compared to the device without dopant segregation. If the gate voltage is increased to 1V (corresponding to the strong on-state), the change in current flow is determined by the change of the tunneling distance X_T as shown in Fig. 4.7(b). For holes, the injection is suppressed due to an increased effective SBH because of the n-type highly doped layer. However, with increasing source-drain voltage the large increase of current by hole injection indicates that the segregation length is still not long enough to suppress the hole current and that holes can still tunnel through the drain barrier. In case of lower dopant concentrations, N_{seg}=1×10^{20}cm^{-3} and 5×10^{19}cm^{-3}, as shown in Fig. 4.8(a), the inverse subthreshold slope of the devices does not even reach thermal limit, only the device with a dopant concentration $\geq 2 \times 10^{20}$cm^{-3} and a segregation length of 2nm exhibits an ideal off-state with S=60mV/dec. The higher the dopant concentration and the larger the segregation length, the more on-current the device can deliver. In contrast, the current for hole injection is strongly suppressed. The device with a segregation length of 4nm and an n-type concentration of 2×10^{20}cm^{-3} as is shown in the Fig. 4.8(a) behaves more like a conventional MOSFET.

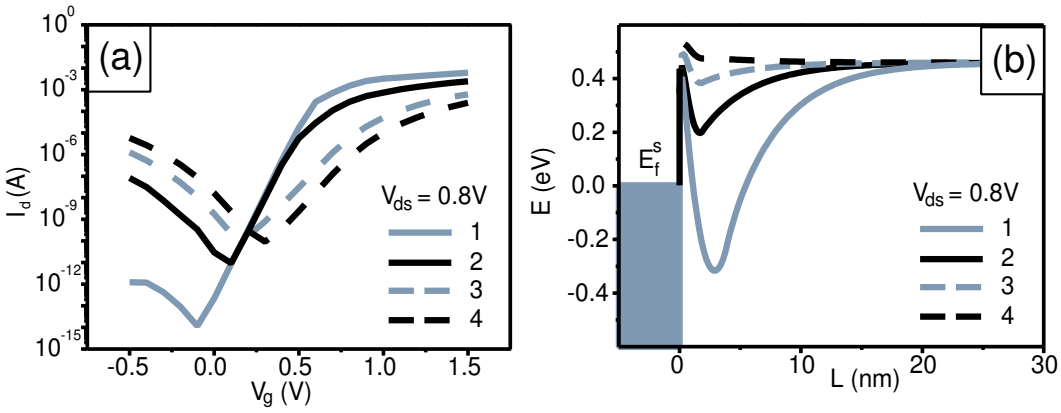


Figure 4.8: (a) Transfer characteristics of SB-MOSFETs with different dopant concentrations N_{seg} and segregation lengths. (b) Energy band diagram at gate voltage 0.1V. 1: N_{seg}=2×10^{20}cm^{-3}, l_{seg} =4nm. 2: N_{seg}=2×10^{20}cm^{-3}, l_{seg} =2nm. 3: N_{seg}=10^{20}cm^{-3}, l_{seg}=2nm. 4: N_{seg}=5×10^{19}cm^{-3}, l_{seg}=2nm.

4.3 Results and discussion

In this chapter we have investigated the impact of gate oxide and channel thickness on the electrical characteristics of fully depleted, single-gated SOI SB-MOSFETs. The simulation results are summarized in Tab. 4.1. These results show that the current control mechanism of SB-MOSFETs is rather different from conventional MOSFETs due to the existence of Schottky barriers at the source and drain contacts. The current transport is dominated by the Schottky barriers instead of the channel itself although scattering in the channel is neglected in the present model. In addition, due to the dependence of the SB width on the gate oxide thickness and the channel thickness, improved on- as well as off-currents have been achieved using an ultra-thin gate oxide and an ultra-thin SOI film because of increased tunneling probabilities. Furthermore, the electrical performance can be significantly improved if a highly doped layer of a few nanometers is incorporated into the device with ultra-thin t_{ox} and t_{si}. Devices with a dopant concentration of N_{seg}=2×10^{20}cm^{-3} and a segregation length of l_{seg} = 2nm show an ideal inverse subthreshold slope of 60mV/dec and on/off-currents comparable to conventional MOSFETs.

Concerning SCE, SB-MOSFETs do not have a better immunity than conventional MOSFETs if both devices are compared at the same current level. Similar to conventional MOSFETs the effective screening length must be

L (nm)	t_{ox} (nm)	t_{si} (nm)	N_{seg} (cm^{-3})	L_{seg} (nm)	S (mV/dec)
30	2	10	-	-	173
60	2	10	-	-	162
60	1.5	10	-	-	150
60	1	10	-	-	134
60	1	8	-	-	122
60	1	6	-	-	112
60	1	4	-	-	94
60	1	6	2×10^{20}	2	60

Table 4.1: Inverse subthreshold slope of the simulated devices (ϕ_{bn}=0.64eV) with different geometrical parameters and dopant segregation.

small enough to suppress SCE. In our case it is 6 times smaller than the gate length. For a future device with a gate length of 10nm, the effective screening length must be less than 1.6nm. In other words, if we use 0.8nm equivalent oxide thickness (EOT), the SOI film must be less than 5nm in order to avoid SCE. Obviously, this is a great challenge for current Si technology since the fabrication of a homogeneous and smooth 5nm ultra-thin SOI layer on large wafers is extremely difficult. If t_{si} is further decreased, vertical quantization and surface roughness can deteriorate the performance of the devices [55]. Double gate and multi-gate device architectures can relax the requirement of ultra-thin SOI because the effective screening length is given by $\lambda = \sqrt{\frac{\varepsilon_{si}}{2\varepsilon_{ox}} t_{si} t_{ox}}$ for double gate devices [56]. Hence, the SOI film thickness can then be twice as large as for single-gated SB-MOSFETs. If t_{ox} is decreased below 0.8nm, direct tunneling through the oxide layer will produce unacceptable large leakage currents [57]. Therefore, alternative gate dielectrics, such as HfO_2 [58, 59] have to be integrated because materials with a large permittivity (high-k) allow a lower EOT compared to silicon dioxide. In addition, the use of high-k materials also relaxes the scaling requirement for the channel thickness because a dielectric with a larger permittivity results in a lower effective screening length λ.

Chapter 5

Schottky diodes

Because the electrical characteristics of the Schottky diodes have a direct impact on the performance of the transistor devices, it is important to gain a deep insight into the operating principle of Schottky diodes. Additionally, optimal parameters for dopant segregation will also be investigated in the Schottky diodes before putting it on the device level.

5.1 Fabrication of Schottky diodes

Schottky diodes on bulk silicon were fabricated in order to study the SBH of silicide-silicon contacts with and without dopant segregation (DS). p-type (100) and n-type (100) bulk silicon wafers with a doping level $\sim 10^{15}\text{cm}^{-3}$ are used for the fabrication of nickel silicide Schottky diodes. As/B was implanted with 20 keV at a dose of $3 \times 10^{15}\text{cm}^{-2}$ into the back side of the n-Si/p-Si. Then, 300nm thermal oxide was grown by wet oxidation at 1050°C for 30 minutes. Subsequently, RIE (reactive ion etching) is used to remove the oxide at the back side and Schottky diode windows were opened by optical lithography and RIE etching at the front side. Next, in order to validate the impact of dopant segregation and to find a good parameter range for dopant segregation, As/B was implanted into the exposed Schottky diode windows at an energy of 15keV and doses ranging from $5 \times 10^{13}\text{cm}^{-2}$ to 10^{15}cm^{-2}. The implantation depths are about 17nm for As and 65nm for B. For standard diodes implantation step was skipped. After removal of the photo-resist and a standard cleaning, the native oxide was etched away directly before nickel deposition. The thickness was adjusted such that the whole implanted Si region was consumed by silicidation (50nm Ni for diodes on n-Si and 80nm Ni for diodes on p-Si). The annealing was performed at 500°C for 90s in a N_2/H_2 (9:1) atmosphere. Unreacted nickel is etched away

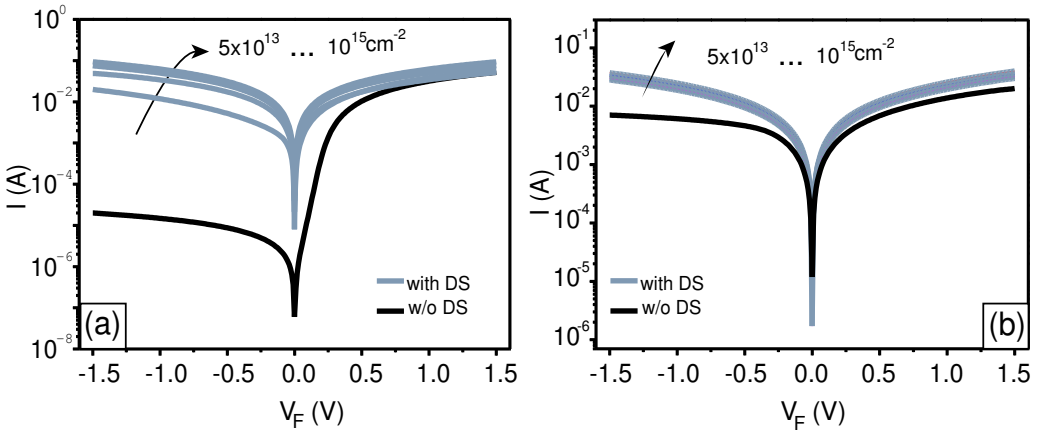


Figure 5.1: (a) $I - V_F$ characteristics of NiSi/n-Si (100) with and without dopant segregation. (b) $I - V_F$ characteristics of NiSi/p-Si (100) with and without dopant segregation. V_F is the applied voltage between the metal and the semiconductor.

by Piranha. The formation of nickel silicide is confirmed using four point electrical measurements and RBS. Finally, aluminum was deposited on the highly doped back-side of the wafer.

5.2 Characteristics of Schottky diodes

Figure 5.1 shows current-voltage ($I - V_F$ curves in black) measurements of NiSi/n-Si (100) as well as NiSi/p-Si (100) Schottky diodes. V_F is the applied voltage between the metal and the semiconductor. The SBH can be obtained from the following equation [23]:

$$\phi_{bn,bp} = \frac{kT}{q} \ln\left(\frac{AA^{**}T^2}{I_s}\right). \tag{5.1}$$

Here, I_s is the reverse saturation current, which can be extrapolated to 0V bias. A is the diode area and A^{**} is the Richardson-constant. The extracted SBH is 0.62eV for electrons and 0.45eV for holes. These values are slightly lower than the SBHs listed in Tab. 2.1. This difference may be attributed to the influence of series resistances and leakage currents.

Schottky diodes with dopant segregation were also characterized by current-voltage ($I-V_F$ curves in gray) measurements. Different curves in gray (shown in Fig. 5.1) represent different implantation doses ranging from $5 \times 10^{13}\text{cm}^{-2}$

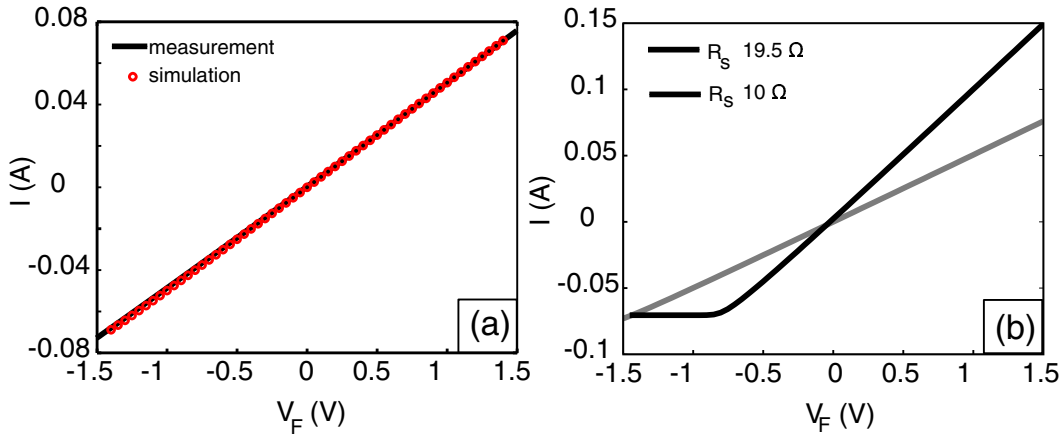


Figure 5.2: (a) Simulated and experimental $I-V_F$ characteristics of NiSi/n-Si (100) with 10^{14}cm^{-2} As implantation. The SBH is ϕ_{bn}=0.37eV and the series resistance is R_s=19.5Ω. (b) shows the impact of the series resistance on the $I-V_F$ characteristics of a Schottky diode.

to 10^{15}cm^{-2}. With increasing implantation dose, the effective SBH of NiSi decreases. At an implantation dose of 10^{14}cm^{-2}, Schottky diodes on both substrates already show ohmic behavior in the measured voltage range as shown in Fig. 5.2(a). Note, that this does not necessarily mean that the effective SBH is very low. The ohmic behavior of the $I-V_F$ curves can also stem from the presence of a rather high silicon series resistance [60]. Simulation results based on Eq. (5.2) in Fig. 5.2(a) show good agreement with measured results with a SBH if 0.37eV and a series resistance of 19.5Ω. However, if an effective SBH lower than 0.37eV is used in the simulation, the $I-V_F$ curves will also exhibit an ohmic behavior. Hence, we still do not know what the real SBH is. Additionally, Figure 5.2(b) shows how the shape of the $I-V_F$ curves is influenced by the series resistance: If the series resistance becomes smaller, a rectifying behavior is clearly observed. In order to obtain the exact SBH, measuring $I-V_F$ curves at lower temperatures and at a larger reverse bias are needed to reveal the difference between the forward and reverse bias data. The extraction of the effective SBH of diodes with dopant segregation will be discussed in detail in the following section.

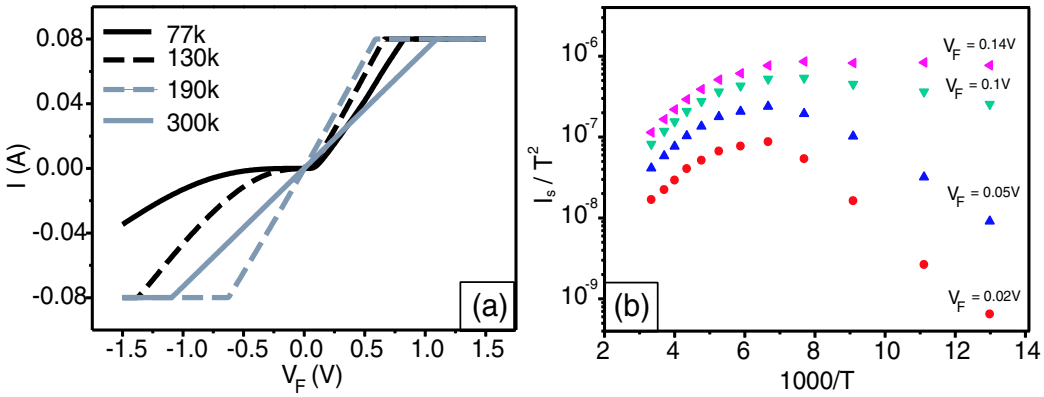


Figure 5.3: (a) Temperature dependent $I - V_F$ characteristics of Schottky diodes with $5 \times 10^{14}\text{cm}^{-2}$ As implantation. (b) Arrhenius plots for the extraction of the effective SBH.

5.3 Low temperature measurements of Schottky diodes

The accurate determination of the SBH of a Schottky contact is always a difficult task when this barrier is very low. The first reason for this is the impact of the series resistance as mentioned in section 5.2 and the other issue is related to the combination of the current transport mechanisms involved including thermal emission and field emission. Figure 5.3(a) shows $I - V_F$ characteristics of a Schottky diode implanted with 5×10^{14}As and measured at different temperatures. Since 80mA is the measurement limit, the current exceeding this value remain constant. Ohmic behavior of the $I - V_F$ characteristics is observed from 300K to 190K. The change of the slope is only due to the temperature dependent series resistance, which is dominant in the measured region. When the temperature is as low as 77K, a rectifying behavior can be seen in the reverse bias, which means that a substantial SB still exists at the Schottky contact. According to the thermal-emission theory, the reverse current of an ideal Schottky diode should saturate at a value of I_s (see chapter 2), but the experiments (Fig. 5.3) show that the current increases for increasing reverse bias. The deviations from the ideal behavior may be caused by a field dependent barrier height and/or field induced tunneling of electrons from the metal to the semiconductor, which can be minimized by the use of a guard-ring [61]. The extracted SBH varies between 0.09 and 0.14eV depending on the forward bias and the temperature range used for

the extraction that lies between 130K and 77K as is shown in Fig. 5.3(b). Note, that this method does not take the impact of the series resistance into account and may lead to a large deviation if the series resistance is much larger than the Schottky contact resistance. Here, we calculated the SBH by numerically computing the current according to the expression:

$$I = AA^{**}T^2 \exp\left(\frac{q\phi_{eff}}{kT}\right)\left(\exp\left(\frac{qV - IR_s}{nkT}\right) - 1\right) \tag{5.2}$$

where R_s is the series resistance that can easily be extracted from the region at large forward bias. For example, in Fig. 5.3(b), the extracted series resistance is 40Ω at 300K but only 10Ω at 77K, a clear evidence of the temperature dependence of the series resistance. In principle, the lower the measurement temperature, the lower the effective SBH that can be extracted by comparing with the numerical calculation (see Eq. (5.2)). For example, for a SBH of ∼0.01eV, a measuring temperature of ∼30K with experimental data is required to see a rectifying behavior in the reverse bias region. However, because the series resistance can become very large at low temperatures due to dopant freezeout (if the silicon is not degenerately doped) and a strong decrease of the carries mobilities [62], it is likely that the $I - V_F$ curves exhibit an ohmic behavior. Hence, the optimal temperature has to be found for these measurements. The ideality factor n is also temperature dependent and can be extracted from the intercept with the y-axis at the zero current according to:

$$\frac{dV}{d(\ln \mathrm{I})} = n\frac{kT}{q} + IR_s. \tag{5.3}$$

Figure 5.4(a) shows the results of simulated $I - V_F$ characteristics at 77K with an effective SBH of ∼ 0.14eV. n is 1.79, which is close to the value extracted from the measurements. The experimentally found temperature dependence of n is shown in Fig. 5.4(b) and yielded n=1.79, 1.63 and 1.57 for 77K, 110K and 150K, respectively. Obviously, n increases with decreasing temperature, which indicates that field emission currents become more important. For the same substrate type and doping, a lower transition temperature between these two regions reflects a lower Schottky specific contact resistance and therefore a lower SBH. The same evaluation of the SBH as above is also carried out for devices with different implantation doses. At an implantation dose of 10^{14}cm^{-2}As, the effective SBH is already reduced to ∼ 0.14eV as shown in Fig. 5.5. Further increasing the implantation dose not lower the SB. On the contrary, the $I - V_F$ characteristics of the diode with an implanted dose of 10^{15}cm^{-2}As is worse than that of the Schottky diode with 5×10^{14}cm^{-2}As, which may be due to the deactivation of dopants. For

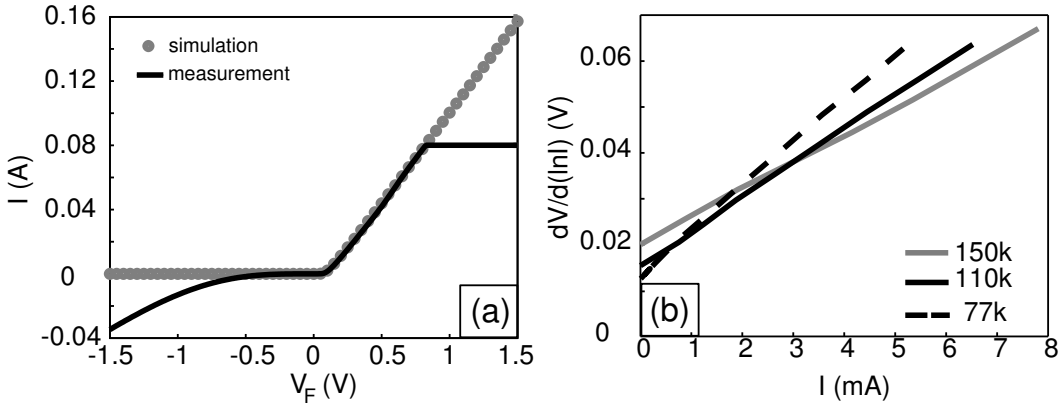


Figure 5.4: (a) Simulated and experimental results of a Schottky diode with $5 \times 10^{14}\text{cm}^{-2}$ arsenic implantation measured at 77K. (b) The experimental $dV/d(lnI)$ versus I plot at different temperatures.

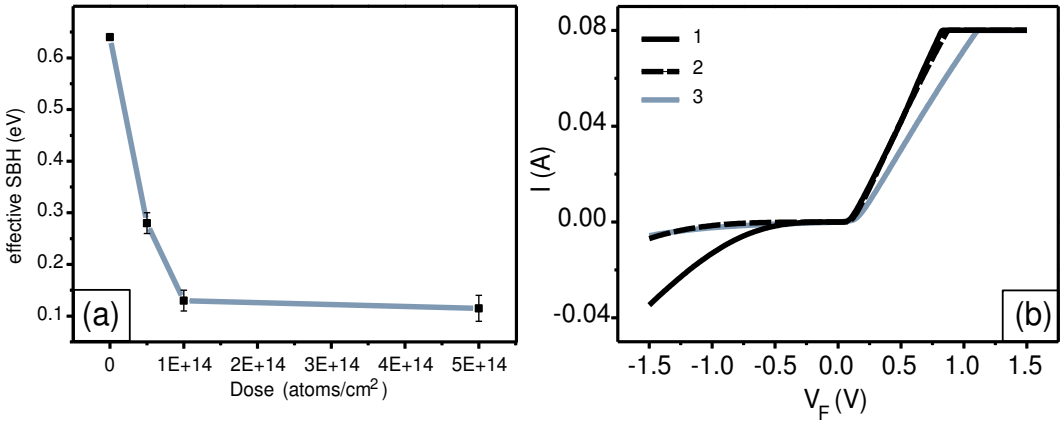


Figure 5.5: (a) Extracted effective SBH at different arsenic implantation doses. (b) $I-V_F$ characteristics of the Schottky diodes with different implantation doses: 1: $5\times10^{14}\text{cm}^{-2}$, 500°C; 2: 10^{15}cm^{-2}, 500°C; 3: $5\times10^{14}\text{cm}^{-2}$, 450°C.

a Schottky diode with an implanted dose of $5 \times 10^{14}\text{cm}^{-2}$As followed by a 450°C for 90s annealing, the transition temperature is higher (210K) than the transition temperature of the sample annealed at 500°C. This may be attributed to the relatively low As concentration in the segregated layer at 450°C.

For Schottky diodes with boron segregation, the temperature dependent measurements show ohmic behavior even at 77K for all devices. From the SIMS measurements shown in chapter 3, one can infer that boron has a concentration only of about $2 \times 10^{18}\text{cm}^{-3}$ at the silicide/Si interface at an implantation dose of $5 \times 10^{13}\text{cm}^{-2}$. This effect, i.e. that no rectifying behavior can be observed even at 77K means that the effective SBH must be very low. A possible explanation of this effect is that the length of the segregated layer is very large. A closer look at the SIMS profiles of boron in chapter 3 confirms that B has a much larger out-diffusion length than As. For a higher implantation energy, the boron out-diffusion may be stronger so that the effective SBH is reduced to approximately zero. However, the dopant segregation behavior might be rather different between the diode devices (vertical direction) and SOI MOSFETs (lateral direction) due to the geometrical constrains. In chapter 7 we will show that SB-MOSFET devices show a clear signature of a residual SB.

Chapter 6

Fabrication of SB-MOSFETs

In this chapter the layout design and the fabrication of SB-MOSFETs will be presented. The emphasis is put on the key processes for ultra-thin SOI, gate oxide growth and short-channel definition by a spacer process.

6.1 Concept of SB-MOSFETs

The concept of SB-MOSFET is based on the simulation results of chapter 4. Devices with ultra-thin gate oxide and ultra-small channel thicknesses in combination with dopant segregation at the silicidation interface between channel and silicide have been fabricated.

6.1.1 Process layout and fabrication

The layout of the SB-MOSFET can be seen in Fig. 6.1(a) for long and Fig. 6.1(b) for short-channel devices. In case of a short-channel device, one additional mask is needed due to the gate patterning by the so-called spacer process [63]. The mask for long channel devices has 4 different gate lengths between $1\mu m$ and $2\mu m$ and 4 different gate widths between $10\mu m$ and $40\mu m$. As a test structure for electron-microscopy investigations lines with $1\mu m$ width and $4\mu m$ distance to each other are implemented into the mask, too. Since the fabrication processes of long- and short-channel devices are similar, the detailed process flow is described together in the following which is illustrated in Fig. 6.2.

(1) Mesa definition
The Mesa is defined by optical lithography (positive M1-Fig. 6.2(a)) and RIE etching after thinning down of the SOI to the desired thickness. $Ar/SF6$

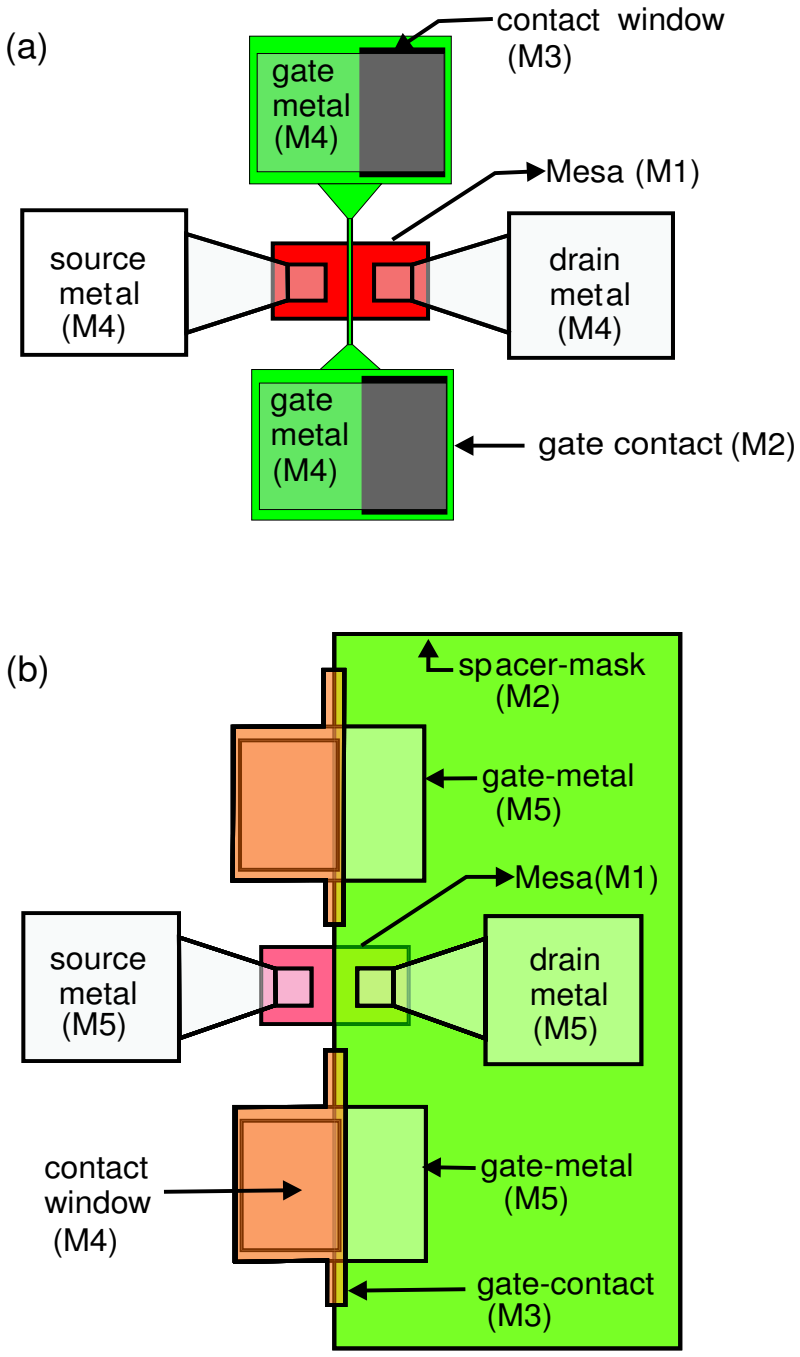


Figure 6.1: Schematic illustration of the mask layout for the fabrication of (a) long-channel SB-MOSFETs and (b) short-channel SB-MOSFETs.

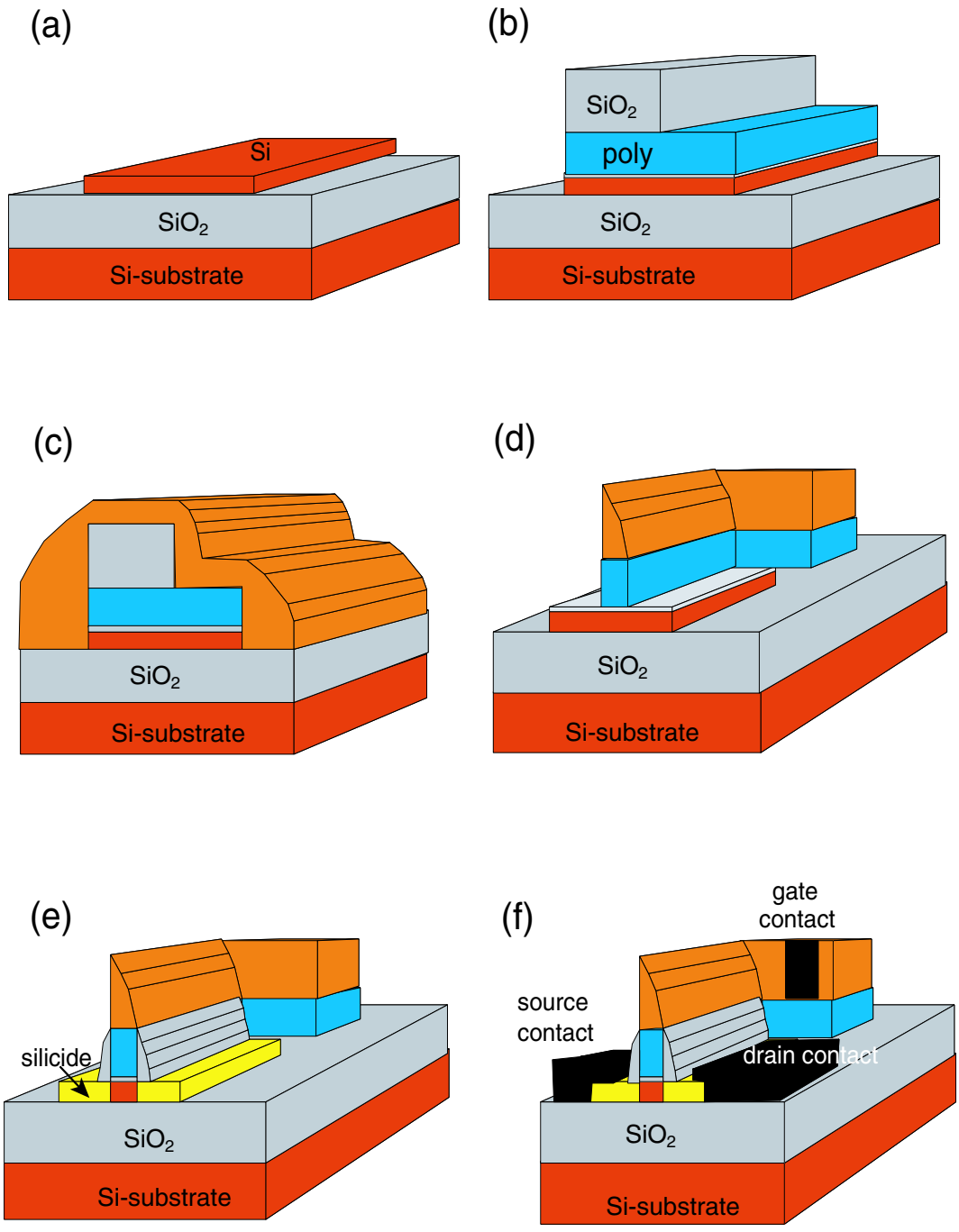


Figure 6.2: Schematic illustration of the fabrication process of short-channel SB-MOSFETs.

Step	time (sec)	HBr flow (sccm)	O_2 flow (sccm)	Bias (W)	ICP (W)	Pressure (mTorr)	Rate (nm/min)
1	10	50	-	50	750	7	60
2	variable	50	2	100	2000	7	variable

Table 6.1: HBr 2-step recipe for poly-etch.

plasma is used to etch the SOI down to the BOX ensuring the isolation of the devices. The mesa has a width of $40\mu m$, $30\mu m$, $20\mu m$, and $10\mu m$, corresponding to the four different gate widths of the devices.

(2) Gate stack deposition
After mesa etching and removal of the photo-resist with acetone and propanol, the sample is cleaned with a full RCA process directly before the gate oxidation. The gate oxide is grown using a low temperature wet oxidation for 1h [66]. After oxidation, 200nm n-type poly-Si and 50nm SiO_2 are deposited by LPCVD. For short-channel devices, 100nm SiO_2 is deposited instead of 50nm. *As* in the poly-Si is activated in an RTA furnace in N_2 atmosphere at 950°C for 1 minute.

(3) Gate stack definition
Long-channel devices: The 50nm SiO_2 on top of the poly-Si is patterned with optical lithography (positive M2-Fig. 6.2(b)) and followed by RIE etching (CHF_3 at 30μbar, 20ml/min, 200W). Then, the sample is cleaned in Piranha ($H_2SO_4 : H_2O_2 = 2 : 1$) at 60°C.

Short-channel devices: The 100nm SiO_2 layer on poly-Si is patterned by optical lithography (positive M2-Fig. 6.2(b)) and followed by RIE etching as above. Then, after the sample is cleaned in Piranha, LPCVD Si_3N_4 is deposited. The Si_3N_4 is used as etching mask (positive M3-Fig. 6.2(c)) for different gate lengths. In our case we use 150 nm of Si_3N_4 to get a ∼110nm wide spacer.

Poly-etching is realized by inductively coupled plasma (ICP)-RIE directly after the removal of the native oxide by DHF dip. The optimal recipe for poly-etching is given in Tab. 6.1.1. The high selectivity between SiO_2 and poly-Si allows an exact etch stop and sharp edges.

4. B/As implantation
Dopant implantation is carried out only for devices with dopant segregation.

In our case, after gate patterning, arsenic is implanted at 5keV with a dose of $5\times10^{14}\text{cm}^{-2}$ leading to an implantation depth of 10nm. This dose turned out to be the optimum dose as was discussed in chapter 5.3. Boron is implanted at 2keV with a dose of $3 \times 10^{15}\text{cm}^{-2}$.

5. Gate spacer formation
After Piranha cleaning, 50nm SiO_2 is deposited (LPCVD) on samples without dopant segregation. For samples with dopant implantation PECVD is used to avoid any diffusion of dopants. Subsequently, the gate spacers are formed with RIE.

6. Gate contact window
Optical lithography (negative M4-Fig. 6.2(d)) is used to pattern the gate contact window. The SiO_2 on top of the poly-Si is etched away by RIE. An oxygen plasma is used to get rid of polymers on the silicon surface.

7. Source/drain formation
After the gate contact window has been opened, samples are cleaned by Piranha again. Directly after a DHF dip for 30s, Ni is deposited by e-beam evaporation. The thickness of the Ni depends on t_{si}. Immediately after Ni deposition, the sample is annealed in $N_2/H_2 = 9:1$ atmosphere. The annealing temperatures and times are chosen to get a minimal encroachment for different devices. The unreacted nickel is selectively removed using Piranha (Fig. 6.2(e)).

8. Metallization of the contacts
The final fabrication step is the metallization of the gate, source and drain contacts with a standard lift-off procedure. Optical lithography (negative M5-Fig. 6.2(f)) is used to open the windows for metallization. The native oxide on the top of the silicide is sputtered away by 15-20s Argon followed by 20nm Cr and 150nm Al deposition. Cr is used for better adhesion of the Al film on the silicide. Finally, the photoresist is removed by acetone and propanol leaving behind the contact pads as shown in Fig. 6.3.

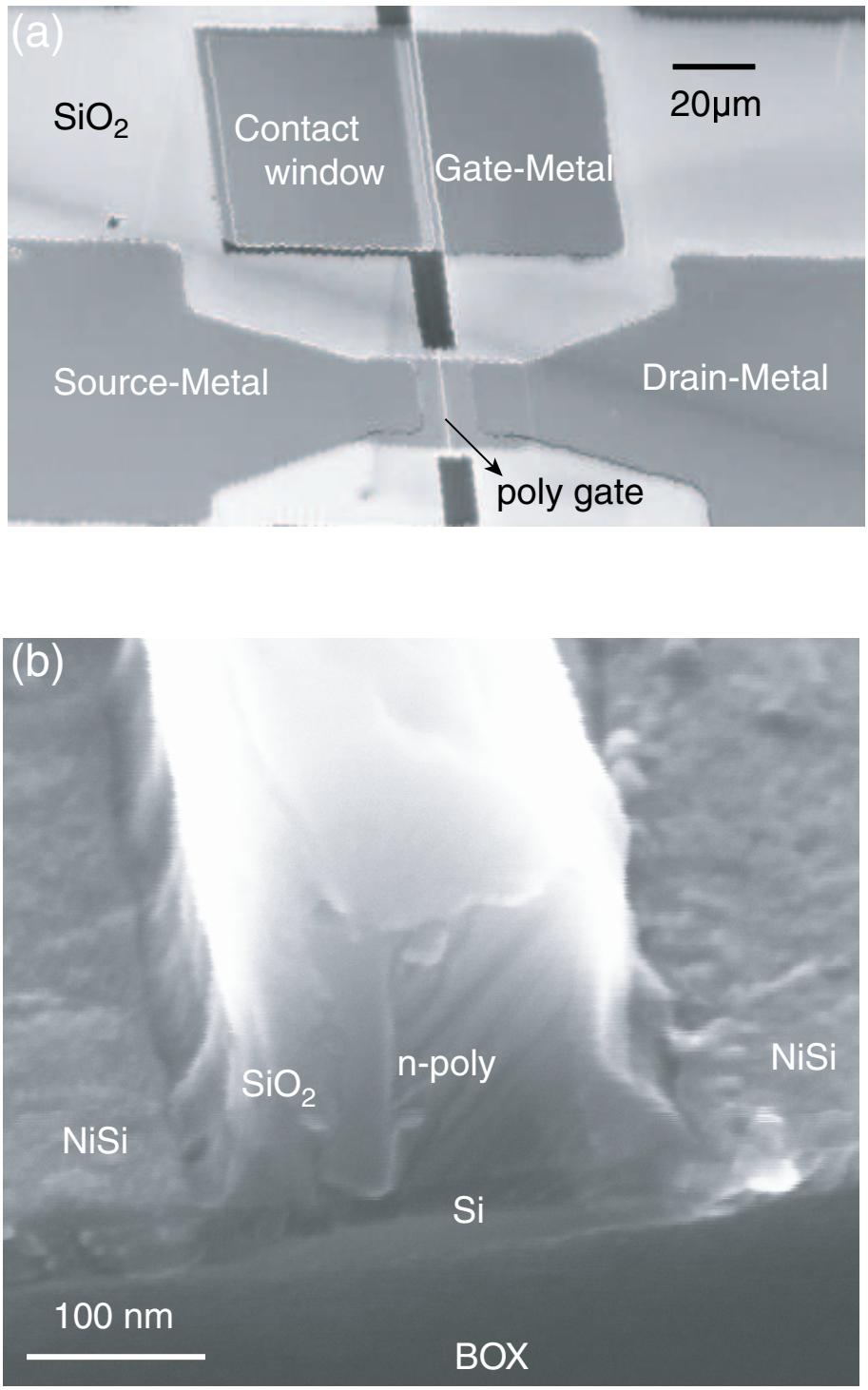


Figure 6.3: SEM images of a SB-MOSFET with a 100nm gate length.

6.2 Process integration

6.2.1 Ultra-thin SOI

As discussed in chapter 4, the use of ultra-thin SOI can reduce SCE and improve the device performance. Although a thin layer of Si on SiO_2 can be made by an adjustment of process parameters during SOI wafer fabrication, there is a limit to how thin the SOI can be. Oxidation thinning or silicon etch back provide two alternative routes to produce thinner SOI. In order to achieve a very controlled thinning of the SOI and avoid roughness of the silicon surface, sacrificial oxidation is used here. In addition, application of a conventional Si surface cleaning procedure helps to get the desired ultra-thin silicon film.

In order to realize ultrathin SOI, 100nm thick, commercially available *p*-type SOI ($N_a = 10^{15}cm^{-3}$) was thinned down to 50nm after 3 hours dry oxidation at 1000°C. The removal of SiO_2 was done by DHF dip with an etching rate of 5-6 nm per minute. After SC2 cleaning, the SOI film was thinned again down to 35 nm using 3 hours wet oxidation at 750°C because of the lower stress and roughness provided by a lower temperature oxidation step compared to dry oxidation at high temperatures [64]. A modified SC1 chemistry with a mixing ratio of 1 : 8 : 64 at 65°C for 10 minutes followed by DHF for oxide removal was used here to thin down to ultra-thin SOI. This optimal ratio can minimize the surface roughness and provides an excellent control over the remaining silicon thickness [65]. Ellipsometry reveals that 1.5nm of silicon is etched away during each SC1/DHF cycle. After several modified SC1 steps, ultra-thin SOI of 10nm was achieved. The loss of silicon during the subsequent fabrication process, i.e. the cleaning before the gate oxidation and the oxidation itself should be taken into account if a certain SOI thickness is desired. Figure 6.4(a) shows an ellipsometry mapping of the SOI wafer after 1000°C dry oxidation and subsequent stripping of the oxide. Obviously, the SOI thickness is very non-uniform with an average thickness of about 53nm and a peak to peak deviation of approximately 10nm. The shape of the SOI film thickness distribution is similar to a Gaussian.

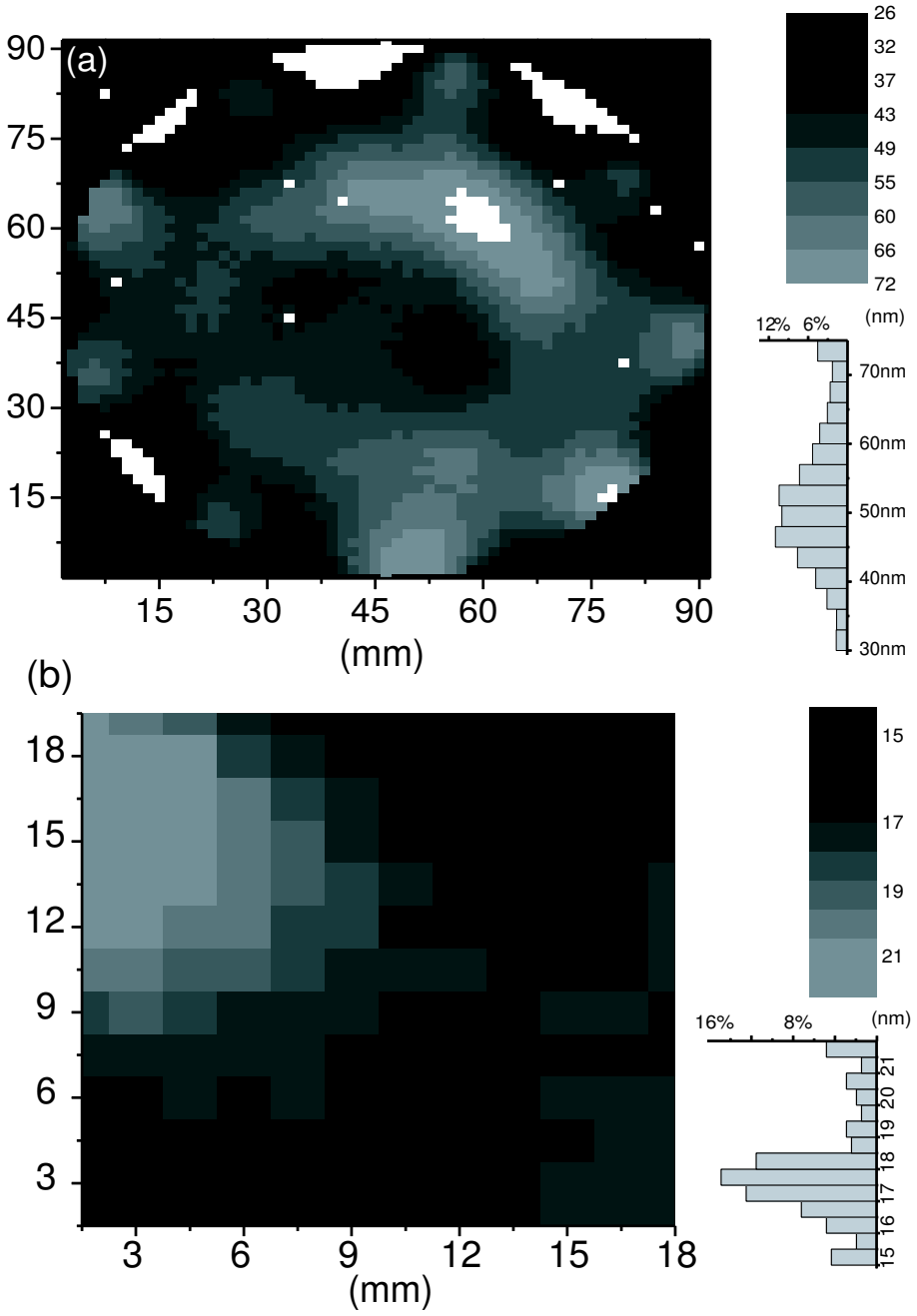


Figure 6.4: (a) Thickness map of a 4″ SOI wafer after 1000°C 3 hours dry oxidation followed by the removal of the grown SiO_2 using DHF (average t_{si}=53nm). (b) Thickness map of a 2cm x 2cm SOI sample after dry/wet oxidation and oxide stripping (average t_{si}=16nm).

6.2.2 Gate oxide

After the mesa isolation, a thin gate oxide is directly grown as dielectric between the gate electrode and the Si channel. In order to lower the roughness of the ultra-thin SOI film, a low temperature gate oxide growth process was used [66]. Dry thermal oxidation uses molecular oxygen rather than water vapor as an oxidant in order to achieve reasonable oxide growth. Temperatures exceeding 600°C are needed. On the other hand, oxide growth at a low temperature can be obtained by wet thermal oxidation.

The wafers are loaded into a glass tube and transferred to the heating zone. During wet oxidation, hydrogen and oxygen gases are introduced into a torch chamber where they react to form water molecules at 950°C then enter the reactor where they diffuse toward the wafers. The water molecules react with the silicon to produce the oxide and hydrogen gas. In our furnace this process produces a ∼3.7nm thick oxide during 600°C wet oxidation for 1h. Devices with other gate oxide thicknesses for comparison are produced also by wet oxidation using slightly different temperatures and times. A low gate current leakage density and a near ideal inverse subthreshold slope of fabricated devices using this oxide growth indicate that the wet thermal procedure yields high quality oxides comparable with high temperature oxides grown in dry oxygen and consistent with the results in Ref. [66].

6.2.3 Elevated source and drain

The salicide process can significantly reduce the sheet resistance of source and drain. But in case of an ultra-thin SOI, the thickness of the silicide will be on the same order as the film thickness itself and thus the sheet resistance may be rather high. In addition, the formation of a metal rich phase in a small contact area may deteriorate the device performance further. In order to achieve lower series resistances, selective epitaxial growth (SEG) or a recessed channel structure are widely used in processing of conventional MOSFETs [67, 68]. Obviously, elevated source and drain can dramatically decrease the series resistance because the cross-section and the thickness of the contact is increased. In addition, metal rich silicide phases can be avoided. Elevated source and drain technology can also be extended to SB-MOSFETs. However, the small contact interface between the silicide and the silicon cannot be avoided because fully silicided source and drain on ultra-thin SOI is needed in order to get a good gate control over the SB contact. The overlap of the gate and source-drain can degrade the transconductance and high-frequency of the device [69]. However, our goal is primarily to gain an optimum control of the SB contact and its barrier height for DC analysis.

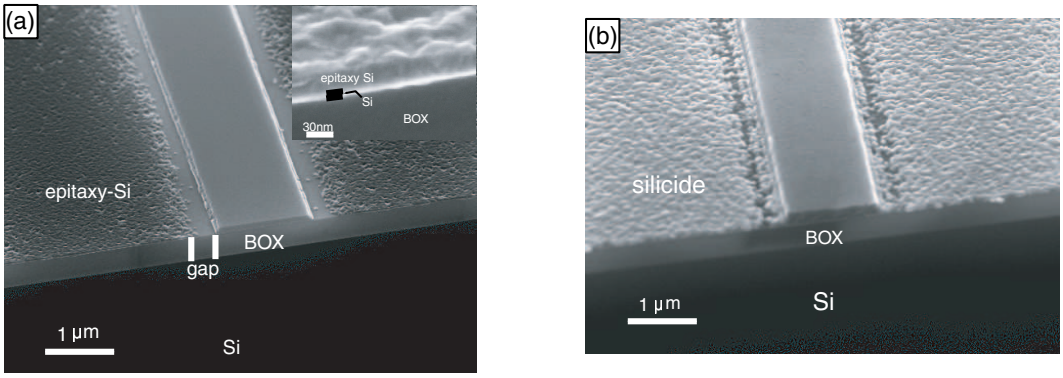


Figure 6.5: (a) SEM of an elevated source-drain test structure. The inset shows a magnification after selective epitaxy, Si thickness increases from 9nm to 30nm (b) SEM photograph after silicidation of an elevated source-drain structure.

Therefore, it is necessary to have the barrier region underneath the gate in order to ensure an equal electrostatic situation in the different devices.

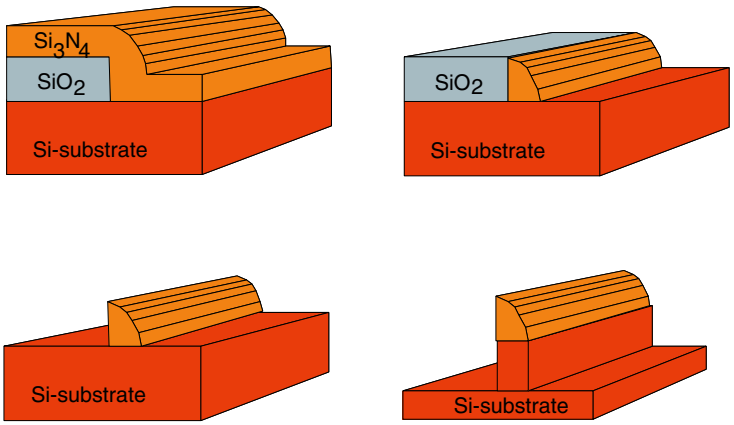
Figure 6.5 shows an SEM image of a test structure after selective epitaxy and after silicidation of the elevated source and drain areas. A gap of approximately 100nm near the gate spacer can be seen in Fig. 6.5(a) indicating that the SEG process is not yet optimized and needs to be further investigated. Because both, the source and the drain contacts are about $10\mu m$ away from the spacer in a real device (see Fig. 6.3(a)), devices with SEG can still dramatically reduce the parasitic resistance of the source and drain extensions and improve the on-current as well as the transconductance if compared to devices without SEG. A more detailed analysis will be given in chapter 7.

6.2.4 Fabrication of 100 nm gate lengths

There are several techniques to fabricate sub-100nm devices with high-resolution patterning such as electron beam lithography, X-ray lithography, extreme ultraviolet lithography etc. Recently, several papers have proposed another attractive way, called spacer patterning to fabricate Si nano-lines using an oxide/nitride spacer as a hard mask [70, 71, 63]. This method can produce uniform lines and is controllable even down to the sub-10 nm region comparable to E-beam lithography . A schematic illustration of the spacer gate process steps and an SEM image of a fabricated test structure is shown in Fig. 6.6. A silicon pillar with ∼50nm width and Si_3N_4 on top can be seen. The edge of the silicon pillar is rather smooth and sharp. In the real device,

the poly-gate is patterned using this spacer process.

(a)



(b)

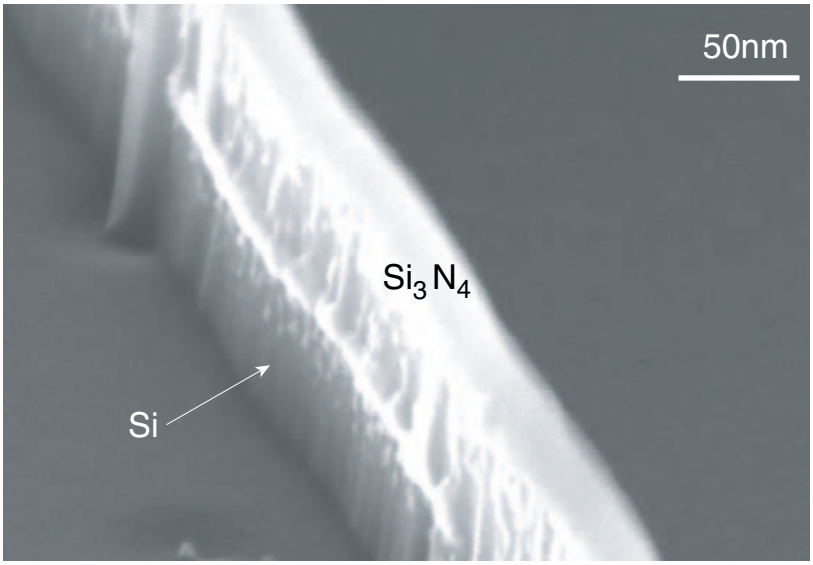


Figure 6.6: (a) Schematic illustration of the spacer gate process for the fabrication of sub-100nm gates. (b) SEM photograph of the cross-section of a sub-100nm gate line fabricated using the technology illustrated in (a).

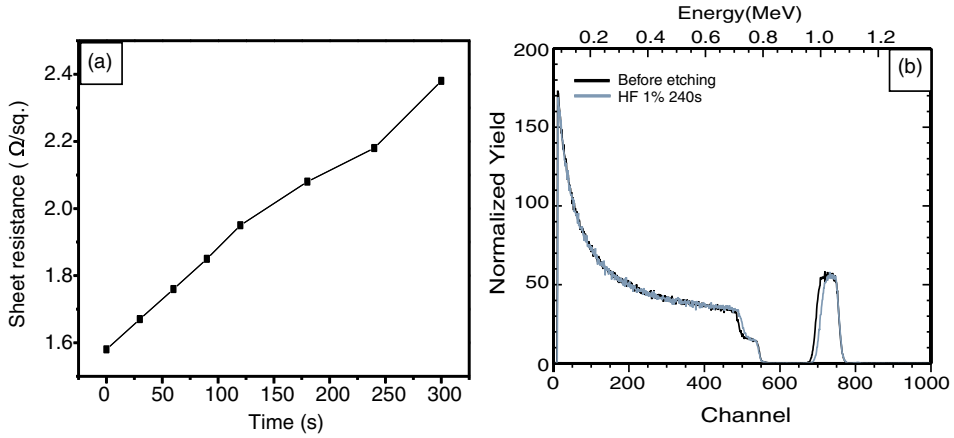


Figure 6.7: (a) The sheet resistivity of a nickel silicide film etched in DHF versus etching time. (b) RBS spectra before DHF and after 240s DHF etch.

6.3 Surface cleaning and etching

The silicide formation critically depends on a proper surface cleaning prior to the silcidation. Impurities such as polymer residues from the gate spacer process or a native oxide may prohibit the formation of a good quality silicide or even lead to a lack of silicidation. Normally, directly before nickel deposition, polymers must be removed by a 10s oxygen plasma and then the native SiO_2 is removed by a DHF dip. Prior to the aluminum deposition, the native oxide on the NiSi has to be removed too, either by 15-20s Argon sputtering or DHF dip. The thickness and sheet resistance of the NiSi layer before and after the DHF dip or sputtering can be investigated by RBS and four point electrical measurements as shown in Fig. 6.7. The etching rate of NiSi was determined from RBS measurements to be about 4-5nm/min in both cases.

Chapter 7

Electrical characteristics of SB-MOSFET

In the present chapter, the electrical behavior of the fabricated SB-MOSFET devices is investigated in detail. Temperature dependent measurements are used to extract the effective SBH of SB-MOSFETs to investigate the factors affecting the SBH. All measurement are performed with a Hewlett Packard semiconductor parameter analyzer 4145B.

7.1 SB-MOSFETs

In this section, we only deal with fully-depleted SOI SB-MOSFETS since the depletion length is much larger than the channel thickness of all devices. Figure 7.1(a) shows subthreshold characteristics of a $2\mu m$ gate length SB-MOSFET at negative source-drain voltage. An ambipolar behavior - typical of SB-MOSFETs - is observed, which agrees well with the simulation results of chapter 4. The n-type branch exhibits a strong DIBL-like behavior at different V_{ds} because of the wrong polarity of the source-drain voltage with respect to the gate voltage as has already been discussed in chapter 2. In the n-channel operation region (towards positive gate bias), the subthreshold slope is $S_{iii)}$=220mV/dec, exceeding 60mV/dec by far because of tunneling being the dominant current mechanism. In the p-channel operation region (towards negative gate bias), two inverse subthreshold slopes can be seen with $S_{ii)}$=70mV/dec and $S_{i)}$=330mV/dec. $S_{ii)}$ is close to the thermal limit meaning that the current in this gate voltage range is determined by so-called bulk-switching, i.e. thermal emission of holes over the potential barrier of the valence band at the source end of the device [32]. For more negative V_{gs} the current eventually is dominated by tunneling through the Schottky barrier

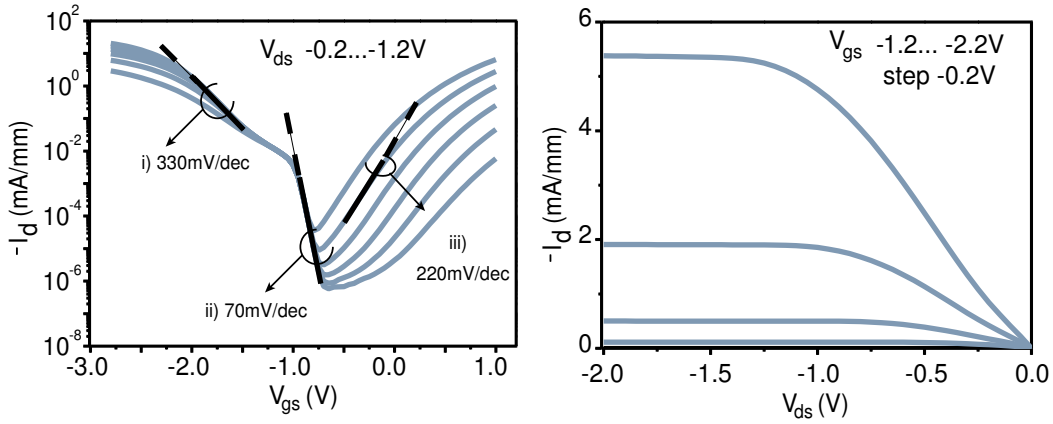


Figure 7.1: (a) Transfer characteristics of a SB-MOSFET at different V_{ds}. (b) Output characteristics at different V_{gs}. The device has a gate length of $2\mu m$ and gate oxide thickness t_{ox}=3.7nm and a channel thickness of t_{si}=50nm.

for holes which manifests itself in a subthreshold slope of $S_{iii)}$=330mV/dec.

Such a behavior with two slopes on one branch of the ambipolar characteristics can be explained by a Fermi level pinning which is not at midgap. For NiSi the Fermi level pinning at the NiSi/Si interface is indeed asymmetric with a barrier for holes of ϕ_{bp}=0.48eV and for electrons of ϕ_{bn}=0.64eV [72]. With increasing source-drain voltage, the range of thermal emission becomes smaller, which is attributed to the tunneling current from the n-branch at the drain contact.

Figure 7.1(b) shows output characteristics of a p-type SB-MOSFET. At low source-drain voltages the curves exhibit a clear sub-linear behavior, which is a signature of a significant SB present at the drain contact. Figure 7.2(a) shows subthreshold characteristics of this device at positive source-drain voltages. The DIBL-like effect is now expected in the p-type operation region and the inverse subthreshold slope for electron injection is 216mV/dec at V_{ds}=1V, almost the same as at V_{ds}=-1V is shown in Fig. 7.1(a). This is expected, since the effect of the V_{ds} polarity on the shape of the SB is compensated by the shift of the gate voltage. Hence, there is no difference for the extraction of S for both cases. Recall that the SBH for electrons in NiSi is about 0.64eV. Hence, if S is extracted at low V_{ds} the value of S will be influenced by the SB formed at the drain contact. As shown in Fig. 7.2(a), the inverse subthreshold slope for electrons decreases for increasing V_{ds} and saturates if V_{ds} is large enough to overcome the SB at the drain contact. Therefore, we use only large V_{ds} to extract S.

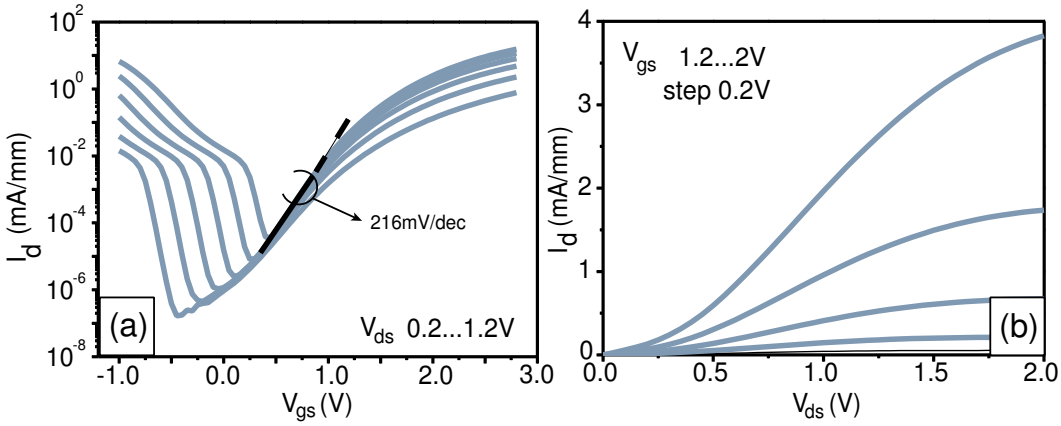


Figure 7.2: (a) Transfer characteristics of a SB-MOSFET at different V_{ds}. (b) Output characteristics at different V_{gs}. t_{ox}=3.7nm, t_{si}=50nm.

If we compare the output characteristics of the electron and the hole branch, the electron branch shows a stronger sub-linear behavior and a much smaller saturation region than the hole branch at the same gate voltage overdrive. This also indicates that the barrier of the electrons is larger than that for holes, which becomes even more significant on p-type SOI substrate for electrons [73].

7.1.1 Exchange of source and drain

On exchanging the source and drain electrodes while keeping the gate and source-drain voltages constant, the device shows a rather different on-current. This phenomena can be explained by the exponential sensitivity of the tunnelling current on the SBH. Therefore, a slightly different SBH at the source and drain contacts results in a rather different drain current [74]. As shown in Fig. 7.3(a), the drain current is four times smaller if source and drain are exchanged because the SBH for holes at the source contact is larger than that at the drain contact in Fig. 7.3(b). However, a closer look at the inverse subthreshold slope shows that it does not change in the thermal emission region, which is expected since the thermal emission region is the region where the valence band is above the barrier anyway and only dependent on temperature according to $S \sim (k_B T)\ln(10)$, with S=60mV/dec for T=300K. In the n-branch, the inverse subthreshold slope is almost the same which indicates that small fluctuations of a high SBH have only little impact on S. In the following sections, only the inverse subthreshold slope for electrons in the

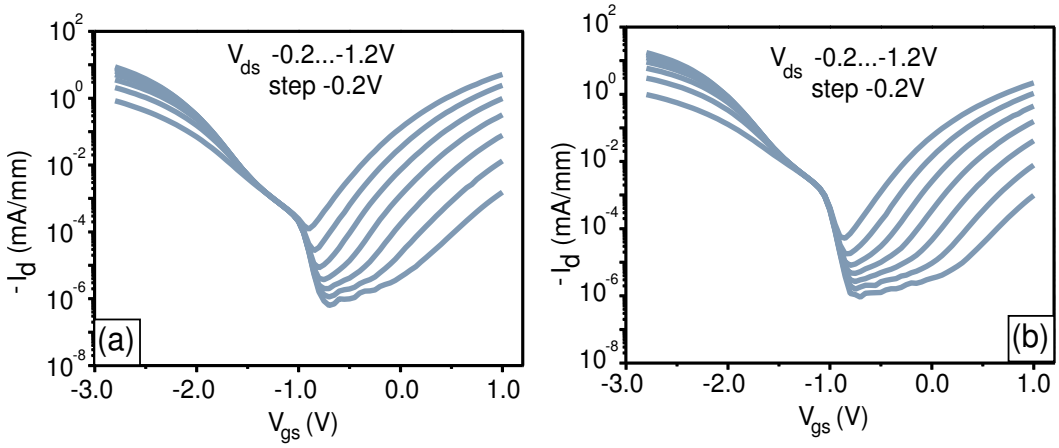


Figure 7.3: (a) Transfer characteristics of a SB-MOSFET at different V_{ds} with t_{ox}=3.7nm and t_{si}=50nm. (b) Transfer characteristics of a SB-MOSFET after source-drain exchange.

n-type branch is investigated because S is not sensitive to the fluctuations in the barrier height. In addition, S is also independent of the source-drain parasitic resistance because the shape of the SB at the source contact is only modulated by the gate voltage induced electrical field.

7.1.2 Impact of channel thickness t_{si}

Devices with different SOI thicknesses enable the investigation of the impact of the channel thickness on the electrical behavior. Figure 7.4 shows transfer as well as output characteristics of SB-MOSFETs with 25nm, 9nm and 7nm channel thickness and the same gate oxide thickness of 3.7nm from top to bottom. The inverse subthreshold slopes $S_{i)}$ for the devices are close to thermal limit (60mV/dec) in a small part of the p-branch. However, the device with a channel thickness of 7nm is most sensitive to the applied source-drain voltage resulting in a much smaller thermal emission region if compared to the other devices. This can be understood by the largest modulation of the Schottky barrier width at the source-drain contacts on the thinnest SOI at the same source-drain voltage. The lowest off-current achieved with the thinnest channel device indicates that a junction as small as possible is preferred in order to suppress off-state leakage. The most striking difference of these devices is the obvious improvement regarding the inverse subthreshold slopes in the n-type operation region. S changes from 216mV/dec for the thickest channel to 157mV/dec for the thinnest one. As discussed in

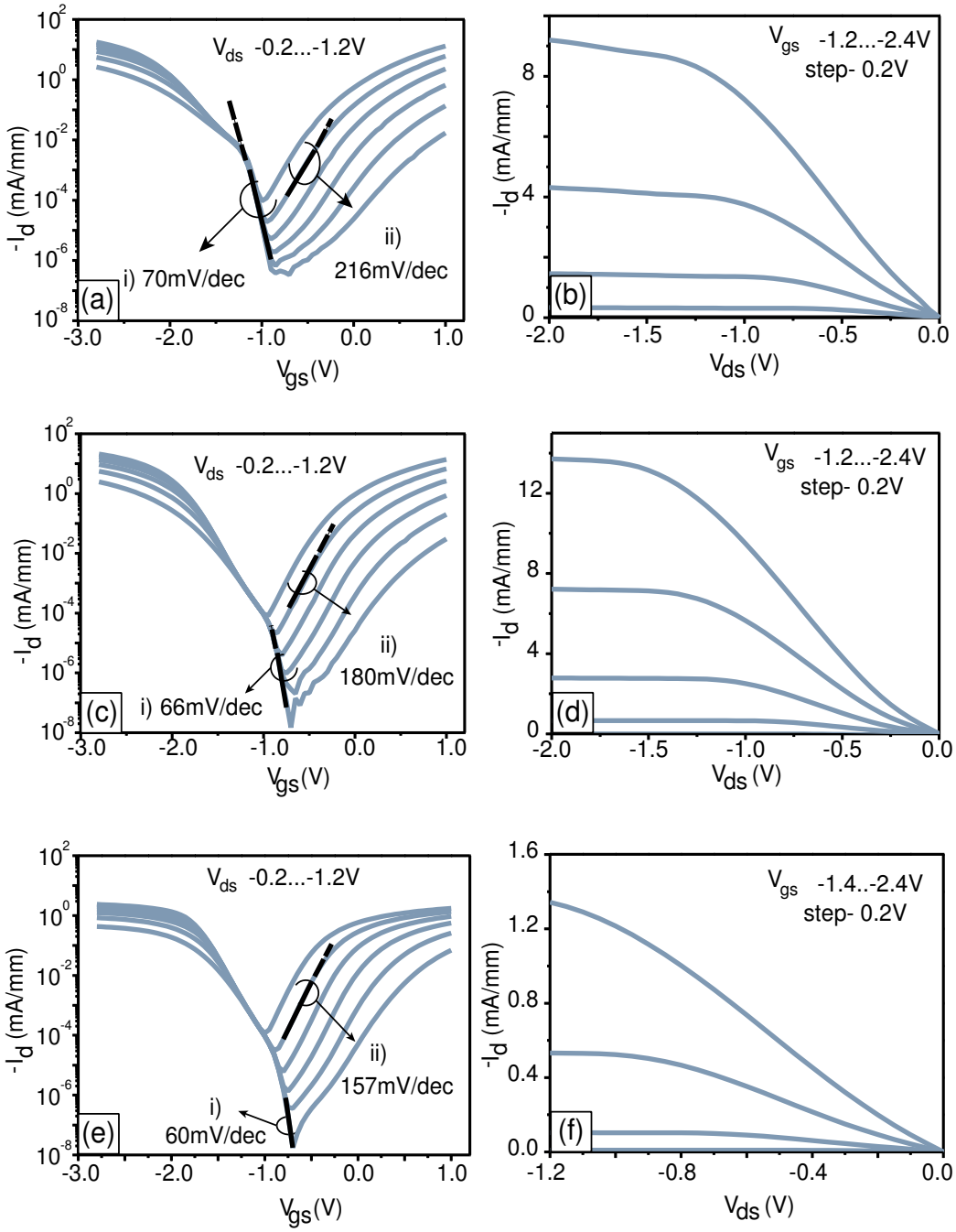


Figure 7.4: Transfer (a)-(c)-(e) and output (b)-(d)-(f) characteristics of devices with the same oxide thickness t_{ox}=3.7nm but with varying t_{si}=25nm, 9nm and 7nm. The gate length is $2\mu m$.

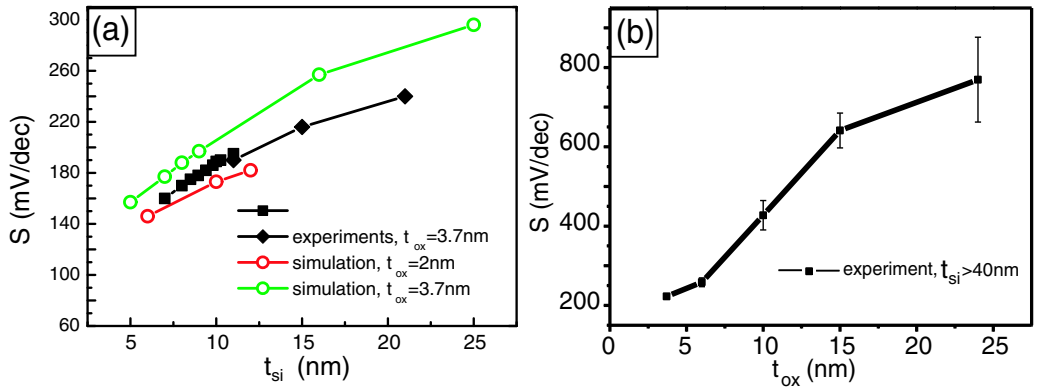


Figure 7.5: (a) Inverse subthreshold slope S versus t_{si}. S becomes smaller with decreasing t_{si}. Experimental and simulated results agree well below t_{si}=25nm but for larger t_{si} the simulated S values exceed the measured one. (b) Inverse subthreshold slope S versus t_{ox}. S becomes larger and sensitive to the fluctuation of t_{si} with increasing t_{ox}.

chapter 4 decreasing t_{si} yields an improved electrical behavior because of a stronger reduction of the effective SBH (due to the stronger gate impact). As a consequence, carriers can more easily tunnel through the source SB. However, the device with 7nm channel thickness has the lowest on-current and g_m, which is due to the ultra-thin silicide film yielding a higher parasitic source/drain resistance compared to the devices with thicker SOI. This problem can be solved by raised source-drain as discussed in section 6.2.3. Therefore, although the gate has a better electrostatic control on device with the thinnest channel thickness, in contrast to simulation results, it does not show the largest on-currents. If the channel thickness is ultra-thin, the electrical performance may be degraded not only due to the high source-drain series resistance but also by other factors, like silicon roughness, electric field fringing by the BOX etc. Hence, a proper selection of the silicon film thickness, the use of a homogenous silicon film and raised source-drain structure should be used to improve the electrical performance.

Figure 7.5(a) shows a comparison of S values between the experimental and simulation results for different t_{si}. With increasing t_{si} thickness (up to ~25nm), S degrades almost by 50%. Exceeding t_{si}=25nm, experimental results show a saturation of S with further increased channel thickness as presented in the former section (t_{si}=50nm, S=230mV/dec). However, the simulated results for the device with t_{si}=50nm has a subthreshold slope of

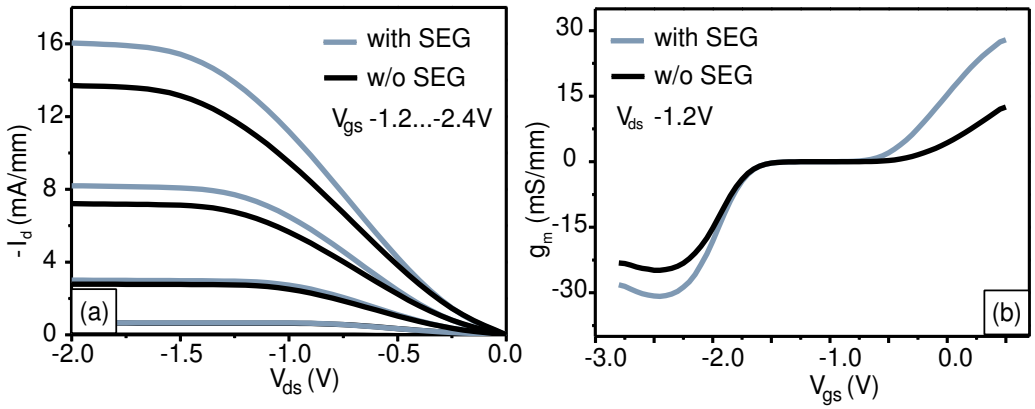


Figure 7.6: (a) Comparison of output characteristics of a device with and without selective epitaxy. (b) Transconductance comparison for device with and without selective epitaxy. The device has a gate oxide thickness of t_{ox}=3.7nm and a channel thickness of t_{si}=9nm.

478mV/dec (not shown). The large deviation at thick Si channels between experimental and simulated results can be attributed to the inexact model because this one-dimensional model is an good approximation only for $\lambda \gg t_{si}$ [75]. On the contrary, the simulation results with t_{ox}=3.2nm and 2nm have a similar shape as the experimental results below t_{si}=25nm. Furthermore, the thinner the Si channel thickness, the closer the results between experiment and simulation.

In order to decrease the high parasitic resistances at source and drain contacts, selective epitaxial growth (SEG) was used. Fig. 7.6 shows output characteristics of a SB-MOSFET and transconductance at V_{ds}=-1.2V before and after SEG. Clearly, because of the reduced parasitic resistance after epitaxy, the on-current and the transconductance are ~20% larger compared to the device without SEG. Recall that the gap between the selective epitaxial growth layer and the spacer still leaves a larger part of the source/drain contact area being unaffected by the raised source/drain as shown in Fig. 6.5. Therefore, after optimization of the SEG process one can expect an even larger improvement.

7.1.3 Impact of gate oxide thickness t_{ox}

Since the inverse subthreshold slope saturates for channel thicknesses exceeding approximately 25nm, we compare the electrical performance of SB-

MOSFET with different gate oxides but thick channels (in our case more than 40nm) and investigate the impact of the gate oxide thickness. This is an appropriate approach since for different oxide thicknesses, in particular if they are large, a larger part of the SOI is consumed and hence this would give an unfair comparison. However, for SOI larger than 25nm in all cases after the gate oxidation a comparison is to a certain degree justified. The inverse subthreshold slope at V_{ds}=-1V increases from 263mV/dec for a device with 6nm gate oxide to 684mV/dec for a device with 16nm gate oxide and the on-current decreases by more than three orders of magnitude, a clear degradation of device performance with an increase of gate oxide thickness. As discussed earlier in chapter 4, as long as the gate leakage is acceptable, devices with Schottky contacts should have a gate oxide as thin as possible. Figure 7.5(b) shows S values of experimental data with different oxide thicknesses. With increasing t_{ox} thickness, S degrades much stronger than the devices with the same t_{ox} but different t_{si} in Fig. 7.5(a). The most striking phenomena is that the measured S value of ≈60 devices on each sample varies in a larger range when t_{ox} increases. Figure 7.8(a) shows the statistical distribution of S values with 24nm t_{ox}. Most S values lie between 600mV/dec and 850mV/dec, almost 40% deviation, which is attributed to the fluctuation of the SOI film thickness. The shape of the S distribution is similar to the distribution of the SOI thicknesses (see thickness mapping of 2x2cm^2 SOI sample of Fig. 6.4). For devices with thin t_{ox} the variation range of S values is much smaller, for example, a device with 3.7nm t_{ox} and 50nm t_{si} has only a 5% variation (not shown), which indicates that the device with thin gate oxide has a good control of the SB and is more tolerant to the non-uniformity of the SOI film. However, if ultra-thin t_{si} is used as shown in Fig. 7.8(b), the variation of S becomes larger again. This effect can be explained by the larger percent of change in t_{si}. All results observed above are consistent with the simulation results in section 4.2.2 and reconfirm the importance of ultra-thin t_{ox} for SB-MOSFETs. In addition, for ultra-thin Si films, SOI with a uniform thickness is desirable in order to avoid the variation of S in SB-MOSFETs.

7.1.4 Impact of dopant segregation

Transfer characteristics of SB-MOSFETs with dopant segregation are shown in Fig. 7.9(a). The device was implanted with 5keV with As^+ ions at a dose of 5×10^{14}cm^{-2} and annealed at 450°C rapid annealing for 20s. The fabricated SB-MOSFET with dopant segregation is shown in Fig. 7.10(a). This device still exhibits ambipolar conduction but now the hole branch is significantly suppressed and the device behaves like an n-type transistor. In

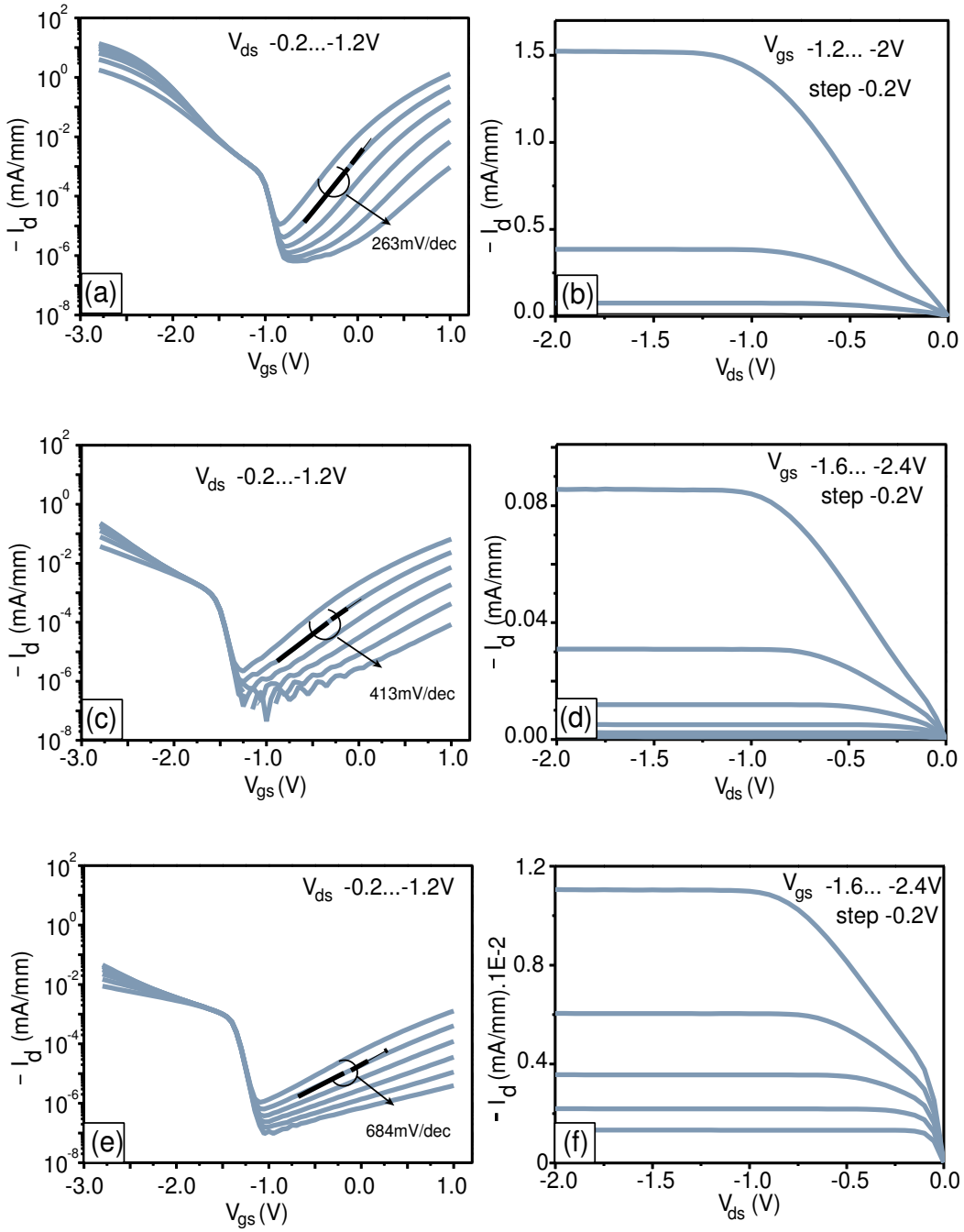


Figure 7.7: Transfer (a)-(c)-(e) and output (b)-(d)-(f) characteristics of devices with t_{ox}=6nm, 10nm and 16nm, respectively.

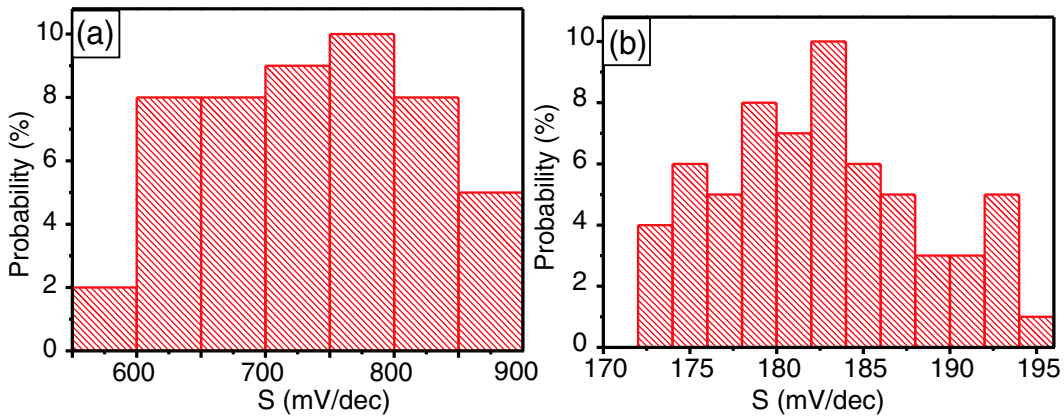


Figure 7.8: (a) Statistical distribution of S for devices with 24nm t_{ox} and thick channel. (b) Statistical distribution of S for devices with 3.7nm t_{ox} and 9nm channel thickness.

addition, the on-current of the electron branch has increased substantially. The most prominent feature of the transfer characteristics, however, is that the inverse subthreshold slope of the n-branch has improved dramatically from ∼216mV/dec to $S_{ii)}$=70mV/dec, nearly approaching the thermal limit. The p-branch now has only one slope with $S_{i)}$=420mV/dec because of tunneling. This means that the device behaves like a bulk-switching, conventional MOSFET which is also reflected in the output characteristics shown in the Fig. 7.9(b). The $I-V$ characteristics do not exhibit an exponential rise of the drain current as often observed in SB-MOSFET devices but show a linear dependence on V_{ds} as conventional MOSFETs. The reason for the change from a p-type to an n-type device is that due to the highly As doped area at the silicide-silicon interface the conduction and valence bands are strongly bent and hence the Schottky barrier for electrons becomes highly transparent. The increased transmission through the Schottky barrier is equivalent to a lower "effective" barrier height, i.e. the effective barrier is strongly reduced and hence the transistor behaves like a conventional n-type device exhibiting a significantly increased drive current. Figure 7.10(b) shows simulation results of the band bending for three different gate voltages representing the p-type operation, the off-state and the n-type operation regions for a transistor with dopant segregation. As mentioned above, the highly doped region at the contact interfaces makes the Schottky barrier very thin such that the bulk potential inside the channel determines the current flow in the off-state (see curves in gray). If the applied gate voltage becomes more positive (see

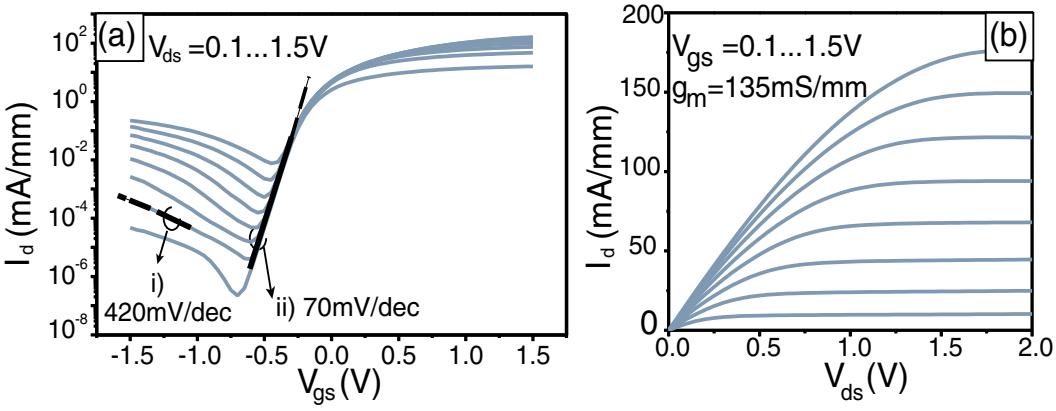


Figure 7.9: (a) Transfer characteristics and (b) Output characteristics of a SB-MOSFET with arsenic dopant segregation. Device has a channel length of $L = 1\mu$m and a channel width of $W = 40\mu$m. The device exhibits n-type characteristics with an inverse subthreshold slope in the n-branch close to the thermal limit.

curves in black dotted line), the conduction band is pushed down and finally the n-type operation region sets in. At the drain side, hole injection from the drain contact stops because the gate voltage increases the SB width for holes so that no holes can penetrate the barrier. On the other hand, a more negative gate voltage (see curves in black) pushes the valence band up. Although an n-type highly doped layer leads to a increased effective SBH for holes, the current on the p-side is still relatively large compared to a conventional MOSFET. This indicates that the spatial extension of the dopant segregation layer can be only a few nanometers so that the holes can still penetrate the increased SB at the drain contact in agreement with Ref. [76, 77]. As already mentioned above the strong band bending situation yields to Schottky barriers with significantly reduced effective SBH. This effect yields steep subthreshold slopes as has been shown experimentally. A similar behavior was observed in case of boron doping as shown in Fig. 7.11. Boron was implanted into the contact areas with an energy of 2keV at a dose of 3×10^{15}cm^{-2} and the device was subsequently annealed at 450°C for 30s. Now, holes can easily be injected into the channel through the thinned Schottky barrier at the contact channel interface. However, in the present case, the doping concentration for B is sufficient to decrease the effective SBH in order to allow for an almost ideal off-state, but the exponential increase of the output characteristics for small bias indicates that a substantial barrier is still present at

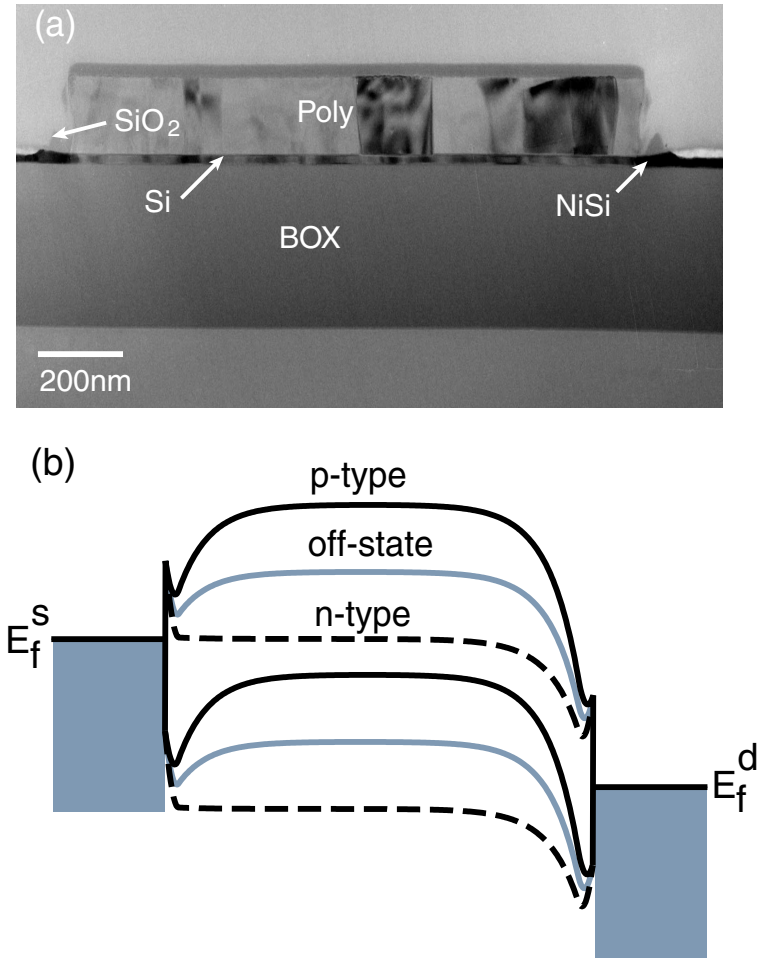


Figure 7.10: (a) TEM image of a fabricated SB-MOSFET with dopant segregation at the silicide/Si interface. (b) Energy band diagram for a SB-MOSFET with dopant segregation under three different gate voltages and a drain voltage of 1V.

the silicide/Si interface. A somewhat higher initial implantation dose would be required in order to increase the B concentration in the segregation layer.

7.2 Low temperature measurements

Temperature dependent measurements were performed in order to study the influence of the geometrical parameters and the dopant segregation on SB-MOSFETs in more detail. The following 2D thermionic emission equation is

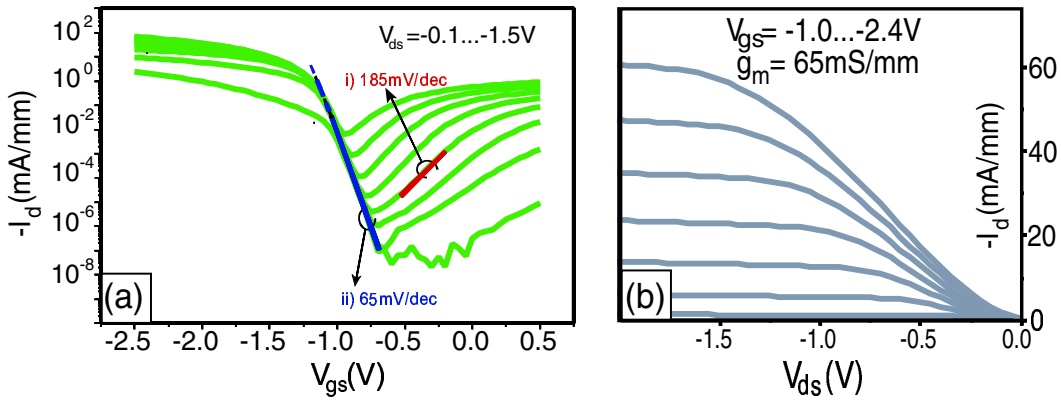


Figure 7.11: (a) Transfer and (b) output characteristics of a SB-MOSFET with boron dopant segregation. The device has a gate length of $L = 1\mu$m and a gate width of $W = 40\mu$m. The device exhibits p-type characteristics with an inverse subthreshold slope in the p-branch close to the thermal limit.

used to extract the SBH from the measured data [78]:

$$I = WA^{**}T^{3/2}\exp(-q\phi_{eff}/kT)\{\exp(qV_{ds}/kT) - 1\} \tag{7.1}$$

where ϕ_{eff} is the effective SBH , W is the channel width, and A^{**} is the 2D effective Richardson constant.

First, we discuss devices without dopant segregation: In Fig. 7.12(a), the device with the thickest t_{ox} and t_{si} has the largest inverse subthreshold slope in the subthreshold region. With a decrease of either of these two parameters, the inverse subthreshold slope becomes smaller. Figure 7.12(b) shows the extracted SBH of electrons at V_{ds}=1V for different geometrical parameters. Due to the different location of the subthreshold region of each device, we choose only the region which we use to extract the inverse subthreshold slope, because the subthreshold region corresponds to the highest sensitivity of a change of the effective SBH with gate voltage for SB-MOSFETs. With a decrease of t_{ox} and/or t_{si}, the SBH change in the subthreshold region becomes more sensitive, which indicates that a SB-MOSFET with ultra-thin t_{ox} and t_{si} is expected to have the best switching behavior. Beyond the threshold voltage, the effective SBH change slows down. This can be understood by a relatively low sensitivity of the effective SBH to the gate voltage. Figure 7.12(b) shows the extracted effective SBH from the Arrhenius plot. The temperature range between 300K and 230K is used for the extraction of the effective SBH.

Now we investigate the device with dopant segregation: Figure 7.13(b)

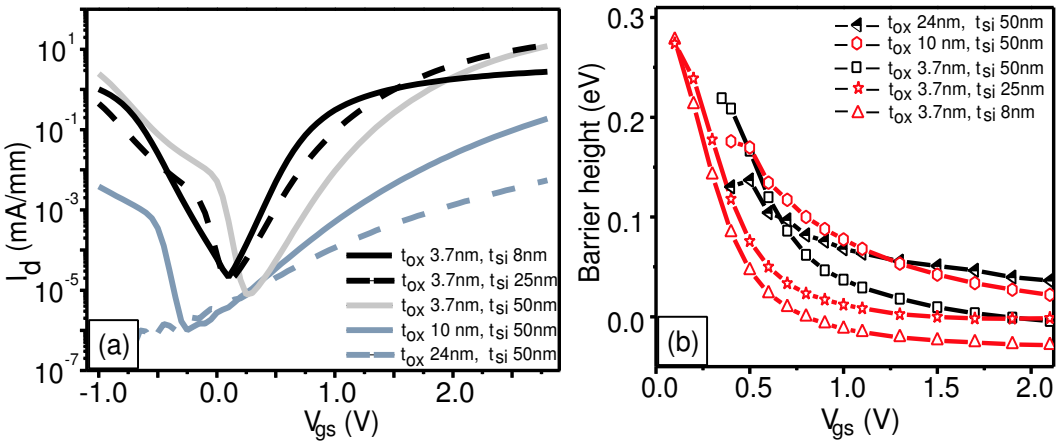


Figure 7.12: (a) $I-V$ characteristics of SB-MOSFETs with different geometrical parameter sets at V_{ds}=1V. (b) Extracted effective SBH for electrons based on the temperature dependent measurements.

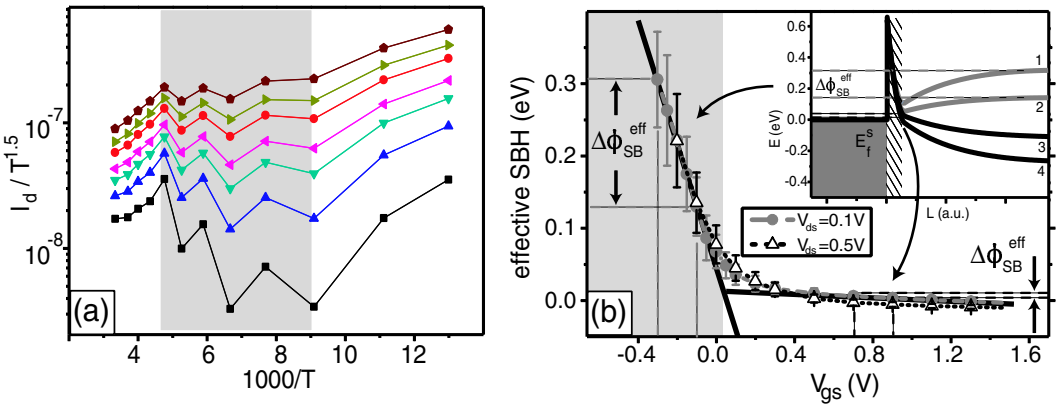


Figure 7.13: (a) Typical Arrhenius plots used for extraction of effective SBH (shadowed area 210K-110K). (b) Extracted effective SBH as a function of V_{gs} at V_{ds}=0.1V (gray circles) and 0.5V (triangles) for electron injection; the error bars result from the uncertainty in determining the slope from the Arrhenius plots. The SBH exhibits a one-to-one change (see the slope in the shaded area) with increasing V_{gs} in the subthreshold region, but a much smaller in the strongly-on region. The inset shows calculated conduction band profiles in the subthreshold region (1, 2) and in the device's on-state (3, 4) for two different V_{gs}.

shows the extracted effective SBH as a function of gate voltage at V_{ds}=0.1V (gray circles) and 0.5V (hollow triangles) exhibiting almost the same dependence on V_{gs}. In the device's off-state the effective SBH exhibits an almost one-to-one change with increasing gate voltage (gray shaded area). This behavior can be illuminated in the inset of Fig. 7.13(b) which shows the conduction band profile (calculated using the model of Ref. [32]) at the source contact for different V_{gs}. The gray curves (denoted 1 and 2) are the conduction band for two different gate voltages in the device's off-state. It can be seen that due to dopant segregation a strong band bending occurs in the highly doped segregation layer leading to a kink in the conduction band as was already discussed. As a result, a change of V_{gs} leads to the same change of bulk potential due to a highly transparent SB in this V_{gs} range. On the contrary, once the device goes into the on-state (V_{gs}>0.3V), the effective SBH continues to decrease but with a much smaller slope (indicated in Fig. 7.13(b)). The reason for this can also be inferred from the conduction band profile in the inset of Fig. 7.13(b): For large V_{gs} (black curves 3 and 4) the conduction band further away from the source contact is pushed below the kink in the segregation layer essentially leaving behind a reduced SB for electron injection much smaller than the original one. The slightly increasing transparency of this reduced SB with changing V_{gs} on the other hand is due to the thinning of the SB with increasing gate voltage and hence is a consequence of the electrostatic control of the gate over the channel. The reduced SB due to dopant segregation can be extracted from Fig. 7.13(b) which is determined by the point where the ϕ_{SB} curve starts to deviate from the one-to-one behavior, i.e. the point where the character of the effective SB changes from the bulk potential-like behavior to the reduced SB [79]. In the present case the reduced SB is found to be $\sim$ 0.1eV significantly lower than the original SBH of NiSi which is 0.64eV for electron injection. The effective SBH is lower than the extracted value in the Schottky-diode case, which may be explained by a different silicide thickness. Since the solubility of arsenic in nickel silicide is still relatively high and if the silicide/Si interface ($\sim$100nm) is located much deeper than the initial dopant implantation depth (10nm) a considerable reduction of the dopants remain in the silicide leading to a lower concentration of segregated dopants. In case of SB-MOSFETs with dopant segregation, the silicide/Si interface is close to the initial implantation profile (as shown in Fig. 7.10(a)). The transfer characteristics at low temperatures show large differences in the inverse subthreshold slope and dramatically suppressed leakage of the p-side at 77K in comparison with room temperature. For low V_{ds}, the on-current at 77K is smaller than at 300K but is larger than at 300K for high V_{ds}. These two facts are not in contradiction with the data presented by Ref. [80] and Ref. [81]. In case of a low V_{ds}, the SB

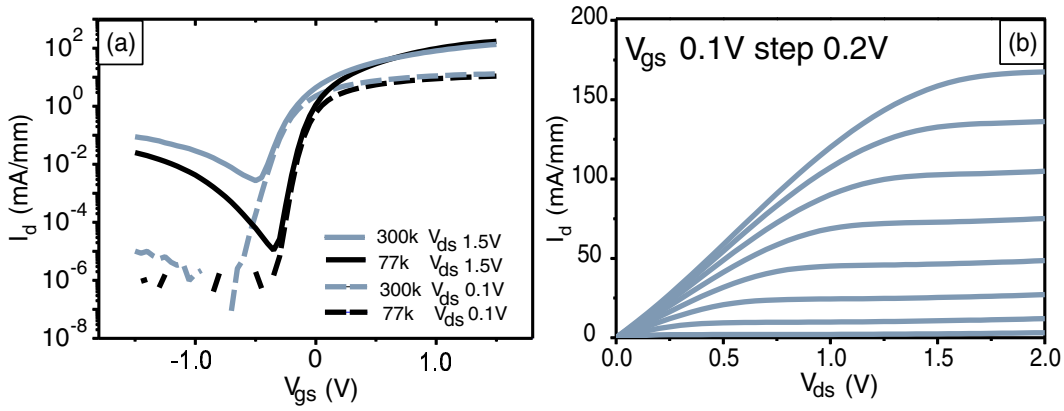


Figure 7.14: (a) Transfer characteristics of a SB-MOSFET with arsenic dopant segregation at different temperature and V_{ds}. (b) Output characteristics at 110K showing a sub-linear effect at low V_{ds}.

presented at the drain contact at 77K is dominant and significantly lowers the drain current (sub-linear effect occurs already at 110K for low V_{ds} as is shown in Fig. 7.14(b)) compared to higher temperature when the device is turned strongly on. On the contrary, if a high V_{ds} is applied, the SB becomes transparent at the drain side and the current is only limited by the channel resistance. Since the mobility at 77K is much larger than at 300K, the current drive is improved. For the devices without dopant segregation, temperature dependent measurements show that the drain current becomes smaller with decreasing temperature even at a large applied V_{ds}, indicating that the SB formed at source and drain is high and the gain from the mobility enhancement at lower temperatures cannot compensate for the loss due to the high SB.

7.3 Short-channel SB-MOSFET

Figure 7.15 shows transfer characteristics of a SB-MOSFET device with a channel length of about 100nm. Because 100nm channel length is still rather large compared to the screening length λ, the inverse subthreshold slope in the thermal emission region is about 83mV/dec at V_{ds}=-0.2V confirming that the device behaves still like a long-channel device. The inverse subthreshold slope in the n-type operation region is 242mV/dec, close to the S value of a 2μ m gate length device, which indicates that S is only dependent on geometrical parameters, namely, the gate oxide and the channel thickness. However,

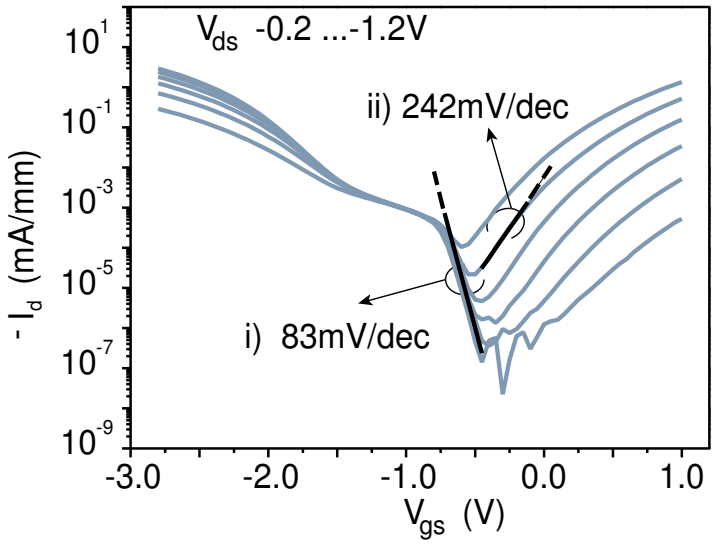


Figure 7.15: Transfer characteristics of a SB-MOSFET with L=100nm W=20μm.

with increasing source-drain voltage the inverse subthreshold slope becomes worse. This suggests a poor gate control of the channel because there is a gap between the silicide and the channel (see Fig. 6.3) and the Schottky contact is not directly under the gate. The smaller on-current of the short-channel device than long-channel device with the same t_{ox} and t_{si} suggests that the gap increases the series resistance significantly and deteriorates the device performance. Short-channel devices with dopant segregation at the silicide/Si channel interface are expected to show a better device performance because of a reduced scattering in the channel compared to the long-channel device with dopant segregation. Such devices will be fabricated and investigated in the future.

7.4 Results

In chapter 7, experimental results of SB-MOSFET devices were presented. In particular, the influence of the SOI film and gate oxide thickness and dopant segregation on the electrical behavior of SB-MOSFETs has been studied. In addition, temperature dependent measurements were also performed to investigate the factors affecting the effective SBH. The most important results can be summarized as follows:

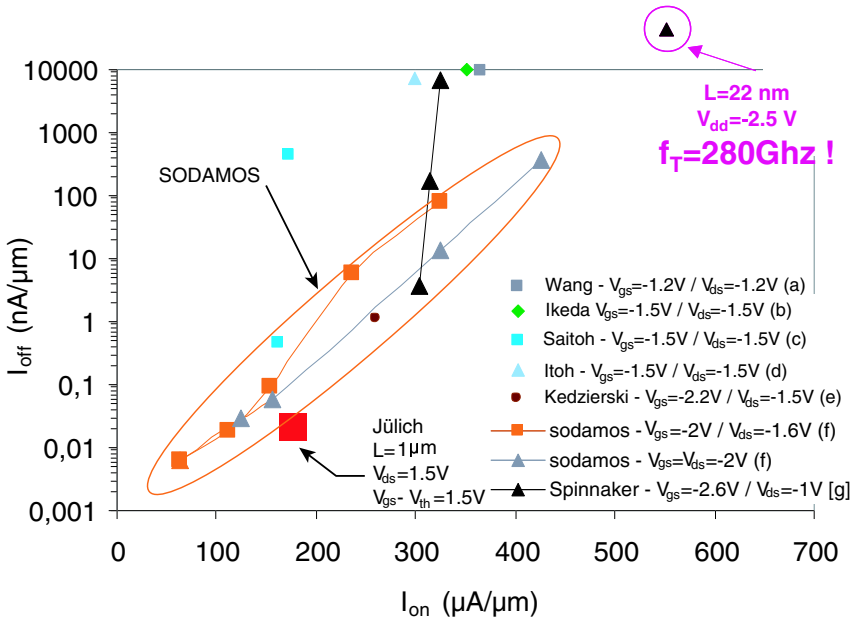


Figure 7.16: Comparison of state-of-the-art SB-MOSFETs of different research groups. The Jülich SB-MOSFET with dopant segregation shows a comparable device performance. (a): Ref. [82], (b): Ref. [83], (c): Ref. [84], (d): Ref. [85], (e): Ref. [5], (f): Ref. [86], (g): Ref. [13].

- The use of ultra-thin t_{ox} and t_{si} improves the switching behavior of SB-MOSFET significantly. The inverse subthreshold slope changes from ∼750mV/dec for a SB-MOSFET with t_{ox}=24nm and thick t_{si} (>40nm) to ∼160mV/dec for a SB-MOSFET with t_{ox}=3.7nm and t_{si}=7nm.

- Using dopant segregation at the silicide/Si channel interface both n-type and p-type SB-MOSFETs with ideal inverse subthreshold slope and strongly improved on-currents have been realized. Temperature dependent measurements show an effective SBH ∼ 0.1eV for electron injection, significantly lower than the original SBH of NiSi of 0.64eV. The tunneling current of holes becomes large with increasing V_{ds} indicating that the highly doped segregation layer has only a length of a few nanometers, which enables a further down-scaling of transistor dimension even to deca-nanometers region.

The comparison of the on-current between the experimental and simulated results (not shown) for device with dopant segregation shows a relatively large deviation indicating that the scattering in a long-channel device becomes serious if SBH is low. In contrast, the experimental results of a long-channel device with high SB agree well with simulation results, in spite of the assumption of a ballistic transport. Figure 7.16 shows the state-of-the-art SB-MOSFETs of different research groups. The present SB-MOSFET device with dopant segregation has already achieved comparable performance. However, such a device still has an enormous potential for further improved electrical performance. Therefore, future work should focus on the combination of ultra-thin oxides, ultra-thin SOI and dopant segregation into an ultra-short channel SB-MOSFET device to achieve a higher performance.

Summary and outlook

The aim of the present work was to improve the performance of SB-MOSFETs such that their performance becomes comparable to conventional MOSFETs and the inherent advantages of SB-MOSFET devices can be exploited. Two different methods are investigated to achieve this goal: one uses an ultra-thin gate oxide and an ultra-thin SOI, the other uses dopant segregation.

The experiment begins with a fully silicided NiSi SOI SB-MOSFET device with a gate oxide thickness of 24nm (t_{ox}) and a channel thickness of 40 $\sim$ 50nm (t_{si}). The $I-V$ characteristics of such a device show an inverse subthreshold slope of $\sim$750mV/dec. With decreasing gate oxide thickness, the inverse subthreshold slope of SB-MOSFET device improves and reaches 230mV/dec for device with t_{ox}=3.7nm. Varying the t_{si} while t_{ox} is kept constant, the inverse subthreshold slope improves further when t_{si} becomes ultra-thin and reaches S=160mV/dec for device with t_{si}=7nm. The geometrical parameters have a distinguished impact on the performance of SB-MOSFET device, i.e. the thinner the gate oxide and the Si channel, the easier carriers can tunnel through, i.e. the lower the effective Schottky barrier height which is due to a tighter gate control. In addition, with decreasing t_{ox} the fluctuation of inverse subthreshold slope becomes smaller and hence devices with ultra-thin gate oxide have more tolerance to the non-uniformity of the SOI thickness. Our findings indicate that the down-scaling of gate oxide is more important and the SOI film must be very uniform when ultra-thin t_{si} is used.

The experiment is also performed on fully silicided NiSi SOI SB-MOSFET devices with dopant segregation. The devices have t_{ox}=3.7nm and t_{si}=25nm. The devices with dopant segregation still exhibit ambipolar conduction but the hole/electron branch is significantly suppressed and the devices behave like n/p-type transistors with a significantly improved inverse subthreshold slope of $\sim$70mV/dec and an I_{on} / I_{off} ratio of 10^7. The silicidation induces a thin and highly doped area at the silicide-silicon interface which bends the conduction/valence bands strongly downwards to the Fermi-level and hence the Schottky barriers for the carriers become highly transparent. This re-

sults in a reduced effective Schottky barrier height. Temperature dependent measurements show an effective Schottky barrier height ~ 0.1eV for electron injection, significantly lower than the original Schottky barrier height of NiSi of 0.64eV. The on-current of such a device amounts to 180mA/mm and the transconductance 135mS/mm with a 1.4V gate overdrive and 2V V_{ds}. These results show drive and leakage currents comparable to state-of-the-art SB-MOSFET devices. However, the fabricated device still has a lot of potential for improvement and for further miniaturization, if the gate oxide and the SOI film thicknesses are decreased. A large tunneling current for holes with increasing V_{ds} in the n-type SB-MOSFET device indicates that dopants at the silicide/Si channel interface are restricted to a few nanometers and such an abrupt junction should enable a further down-scaling of gate length to the deca-nanometer regime.

Simulation results with a self-consistent solution of the one-dimensional modified Poisson and Schroedinger equations for single-gated, fully depleted ballistic SOI-MOSFET show consistency with the experimental findings of the switching behavior, in spite of the assumption of ballistic transport.

Future work will concentrate on a good combination of ultra-thin gate oxide and channel thickness with dopant segregation into an ultra-short channel device to achieve a higher device performance comparable to conventional MOSFETs. In addition, this new technology can now be applied to high mobility channel materials such as strained silicon and high-k gate dielectrics in order to boost the device performance further.

Appendix A

Abbreviation

APM	Ammonia peroxide mixture
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapor deposition
DS	Dopant segregation
HPM	Hydrochloric acid peroxide mixture
ICP	Inductive coupled plasma
LPCVD	Low pressure chemical vapor deposition
MIGS	Metal-induced gap states
MOS	Metal -oxide -semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
PECVD	Plasma enhanced chemical vapor deposition
RBS	Rutherford backscattering spectroscopy
RIE	Reactive ion etching
RTP	Rapid thermal processing
Salicde	Self aligned silicide
SB-MOSFET	Schottky barrier metal-oxide-semiconductor field-effect transistor
SBH	Schottky barrier height
SEM	Scanning electron microscopy
SIIS	Silicidation induced impurity segregation
SIMS	Secondary ion mass spectrometry
SOI	Silicon on insulator
SPM	Sulfuric acid peroxide mixture
TEM	Transmission electron microscopy
UHV	Ultra high vacuum
UTB	Ultra-thin body
XRD	X-ray diffraction
XTEM	Crosssectional transmission electron microscopy

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