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Fakultät für Elektrotechnik und Informationstechnik
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Abschlussbericht zum DFG-Projekt (GZ: Uh53/4-3)

”Untersuchungen zu effizienten asynchronen Schaltungskonzeptionen für Einzelflussquanten-Elektronikschaltungen”

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1. Allgemeine Angaben

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Liste der Publikationen aus diesem Projekt

Papers: (Sonderdrucke beigefügt)

B. Dimov and F. H. Uhlmann, ”New Optimized Elements for the Rapid Single-Flux Quantum Shift Register Family,” *Supercond. Sci. Technol.*, vol.16, pp.1212-1215, 2003

B. Dimov and F. H. Uhlmann, ”High-speed Asynchronous RSFQ Logic Cells with Flexible Gate Delays,” *Proc. 6th European Conference on Applied Superconductivity EUCAS’03*, 14.-18.09.2003, Sorrento, Italy, 2003

B. Dimov, V. Mladenov and F. H. Uhlmann, ”Asynchronous RSFQ Gates with Flexible Delays,” *Proc. 48. Internat. Wiss. Kolloquium, TU-Ilmenau, Germany,* pp.387-388, 2003

B. Dimov, V. Todorov, V. Mladenov and F. H. Uhlmann, ”Optimal Signal Propagation Speed of a Josephson Transmission Line,” *Supercond. Sci. Techn.*, vol.17, pp.819-822, 2004

B. Dimov, V. Todorov, V. Mladenov and F. H. Uhlmann, ”The Josephson Transmission Line as an Impedance Matching Circuits,” *WSEAS Trans. Circuits and Systems*, vol.3, No.5, pp.1341-1346, 2004

B. Dimov, V. Todorov, V. Mladenov and F. H. Uhlmann, ”Possible Connections of the Josephson Junctions within the RSFQ Logic Circuits,” *WSEAS Trans. Circuits and Systems*, vol.3, No.5, pp.1398-1402, 2004

B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer and F. H. Uhlmann, ”Tuning of the RSFQ Gate Speed by Different Stewart-McCumber Param-

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B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer, Th. Ortlepp and F. H. Uhlmann, "Investigation of the Parasitic Coupling Effects in Densely Packaged RSFQ Logic Circuits," *IEEE Trans. Appl. Supercond.,* accepted for publication

B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer and F. H. Uhlmann, "Asynchronous RSFQ Demultiplexer Based on Dual-Rail Information Coding," *Supercond. Sci. Technol.*, submitted for publication

Talks:

B. Dimov and F. H. Uhlmann, "Asynchronous Logic - an Opportunity for Realization of Ultra High-Speed RSFQ Circuits", *SCENET-Meeting March 2003,* 21.-22.03.2003 Teneriffa, Spanien

B. Dimov, V. Mladenov and F. H. Uhlmann, "Asynchronous RSFQ Gates with Flexible Delays," *48. Internat. Wiss. Kolloquium der TU Ilmenau,* 22.-25.09.2003, Ilmenau, Germany

B. Dimov, V. Todorov, V. Mladenov and F. H. Uhlmann, "The Josephson Transmission Line as an Impedance Matching Circuits," *8th WSEAS Internat. Multiconf. Circuits, Systems, Communications and Computers CSCC2004,* Athens, Greece, 2004

B. Dimov, V. Todorov, V. Mladenov and F. H. Uhlmann, "Possible Connections of the Josephson Junctions within the RSFQ Logic Circuits," *8th WSEAS Internat. Multiconf. Circuits, Systems, Communications and Computers CSCC2004,* Athens, Greece, 2004

B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer and F. H. Uhlmann, "Tuning of the RSFQ Gate Speed by Different Stewart-McCumber Parameters of the Josephson Junctions," *Applied Superconductivity Conference ASC/04,* 3.-8.10.2004, Jacksonville, USA

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B. Dimov and F. H. Uhlmann, "High-speed Asynchronous RSFQ Logic Cells with Flexible Gate Delays," *6th European Conference on Applied Superconductivity EUCAS'03,* 14.-18.09.2003, Sorrento, Italy

B. Dimov and F. H. Uhlmann, "New RSFQ Shift Registers for Synchronous and Asynchronous Applications," *Tagung Kryoelektronische Bauelemente KRYO'03,* 5.-7.10.2003, Blaubeuren, Germany

J. Weber, Th. Ortlepp, F. H. Uhlmann, "Untersuchungen der Schalt- und Verzoergungszeiten einer supraleitenden Hochgeschwindigkeitselektronik im Pikosekunden-Bereich," *Tagung Kryoelektronische Bauelemente KRYO'03,* 5.-7.10.2003, Blaubeuren, Germany

B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer and F. H. Uhlmann, "Asynchronous RSFQ Demultiplexer Based on Dual-Rail Data Coding," *Tagung Kryoelektronische Bauelemente KRYO'04,* 12.-14.09.2004, Goslar, Germany

B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer, Th. Ortlepp and F. H. Uhlmann, ”Investigation of the Parasitic Coupling Effects in Densely Packaged RSFQ Logic Circuits,” *Applied Superconductivity Conference ASC/04,* 3.-8.10.2004, Jacksonville, USA

B. Dimov, M. Khabipov, D. Balashov, C. M. Brandt, F. Im. Buchholz, J. Niemeyer and F. H. Uhlmann, ”Asynchronous RSFQ Cell Library Based on Dual-Rail Information Coding,” *336. Wilhelm und Else Heraeus-Seminar*, 29.11.-01.12.2004, Bad Honnef, Germany

Internet presentation:

www-alt.tu-ilmenau.de/EI/ATE/kryo/asyn/index.htm

2. Arbeits- und Ergebnisbericht

2.1. Motivation and Goals of the Project

The continuous growth of the computational power of the modern computers is accompanied by two factors, currently limiting the progress of the high-integrated semiconductor devices:

- The heat power dissipated from the chip becomes extremely large [1];
- The wave length of the global clock signal becomes comparable to the chip size. The interconnect delays start to dominate over the gate ones and serious synchronization problems occur [2].

A possibility to overcome the first problem is given by the Rapid Single Flux Quantum (RSFQ) technique, [3], [4]. The switching element of this logic is the Josephson junction, dissipating dynamic power much less than 10^{-18} J/bit, while the signals are propagated through superconductive (i.e. lossless) transmission lines. Thus, digital circuits with extremely low power dissipation can be fabricated [5].

The second problem can be efficiently overcome by means of the asynchronous logic [6]. An asynchronous circuit is a digital circuit, in which each component reacts to changes on its inputs as these changes arrive, and produces changes on its outputs when it concludes its computation. The coordination between the circuit components is performed locally by some kind of handshaking protocol. No clock signal is provided to synchronize the work of the circuit components, thus avoiding all negative effects originating from the global clocking.

The object of this project is the development of a concept about the implementation of the asynchronous approach within the RSFQ technique. Thus, extremely high-speed complex digital RSFQ circuits with ultra low-power consumption can be developed. Based on this concept, a complete RSFQ cell library is designed, supporting the high-level synthesis of complex asynchronous RSFQ digital devices. A detailed description of the properties of the library components can be found in [7].

2.2. Description of the Concept for Development of Asynchronous RSFQ Digital Circuits

The first phase of the project work has been the choice of the proper type of data coding and handshaking protocol, taking into account the peculiarities of the pulse-based RSFQ technique. The Dual-Rail (DR) data coding [8] has been chosen for the basis of our concept for development of asynchronous RSFQ digital circuits, because it minimizes the risk for signal competitions, allows the synthesis of delay-insensitive asynchronous circuits and facilitates the inclusion of synchronous components into the asynchronous circuits [9]. Its principle is shown in Fig. 1. Two lines (”true” and ”false”) are used per bit of information that has to

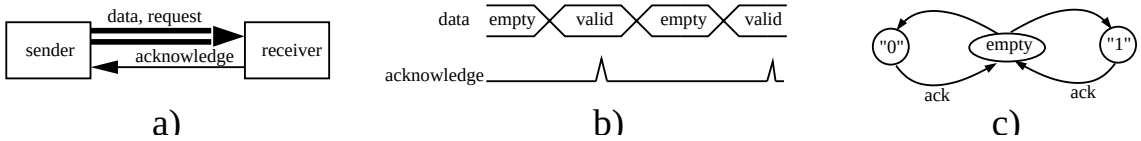

Figure 1. a) Dual-rail channel; b) data flow; c) the equivalent Mealy diagram.

be communicated. Appearance of a signal in the ”true” line is interpreted as a logic ”1”; appearance of a signal in the ”false” line is interpreted as a logic ”0”. These states are named *valid codewords*. No logic signal in both lines is named *empty codeword*, simultaneous existence of signals in both lines is forbidden. The appearance of a valid codeword is considered also as a request signal. A separate channel is provided only for the acknowledge

signal. In this way, the probability for signal races is reduced and the synchronization is internally carried by the data.

An important issue within the developed concept for synthesis of asynchronous RSFQ digital circuits is the modeling of the asynchronous RSFQ gates delays. Generally, the synthesis of delay-insensitive (DI) asynchronous circuits (i.e. asynchronous circuits working for arbitrary delays of their components) is possible with the DR data coding [9], but the resulting circuits topologies are extremely complicated and could be even slower than their synchronous equivalents. Asynchronous circuits with higher speed and much simpler topology result, if their synthesis is based on bounded delay models of the gates. But in case of violation of these boundaries, a wrong logical behaviour of the asynchronous circuit occurs. Therefore, a special attention is paid on the careful definition of the bi-bounds of the gates in the developed asynchronous RSFQ cell library [7].

A paradox characterizing the asynchronous digital circuits is the complicated and nonstraightforward relation between the gates delays and the delay (resp. the speed) of the circuit, composed from these gates. It is not true, that the faster the gates are, the faster the circuit composed from these gates is and an expressive example can be found in [6], pp.3-7. If the topology of a complex asynchronous circuit is already determined, one may optimize the delays of its gates in order to maximize its speed. Therefore, an important advantage of the asynchronous cell library components is the adjustability of their delays. About the semiconductor electronics, such gate delay tuning is impossible - once the gate topology is determined, its nominal delay is fixed and can not be manipulated. This is not the case of the RSFQ technique. An important step of the present research has been the invention of the possible methods for RSFQ gate delay tuning [10], [11]. They are:

- By scaling the dc bias currents of the junctions within the RSFQ gates;
- By scaling the inductances of the lines connecting the junctions within the RSFQ gates;
- By scaling the external shunt resistors of the junctions within the RSFQ gates (named below *the β_c-method*, because thus the Stewart-McCumber parameter β_c of the junctions is manipulated). Note, that this method is applicable only about RSFQ fabrication technologies, based on externally shunted Josephson junctions.

These methods are compared in [10] with respect to their technological realization, effectiveness, influence over the gate compatibility and impact on the gate margins and fabrication yield. There is demonstrated by simulations, that the β_c-method has a straightforward technological realization, no influence over the gate compatibility, high effectiveness and negligible impact on the gate margins and the fabrication yield, thus evaluating it as the best method for tuning the delays of the asynchronous RSFQ gates. This statement is experimentally proven in [11]. The measurements described there fully coincide with the drawn by simulations statement in [10], that the β_c-method has a high effectiveness and negligible impact on the RSFQ gate margins and fabrication yield. Thus, the evaluation of the β_c-method as the best one for tuning the delays of the asynchronous RSFQ gates is experimentally confirmed. Within the proposed concept for synthesis of asynchronous RSFQ digital circuits, this method is pointed out as a powerful tool for RSFQ gate delay manipulation and adjusting.

2.3. Components of the Developed Asynchronous RSFQ Cell Library

The concept about the development of asynchronous RSFQ digital circuits, described above, is implemented into an RSFQ cell library, containing all gates necessary for the high-level synthesis of complex asynchronous RSFQ digital devices. The electrical schemes of all gates are simulated with the commercial transient simulator ELDO [12] and the Josephson junctions are analyzed within the RCLSJ-model [13]. The values of their elements are optimized by

the centers-of-gravity method [14] in order to improve the global margins of the junctions critical currents, the dc bias currents and the inductances, thus maximizing the gate fabrication yield. Next, the optimized electrical schemes of the gates have been implemented into layouts, taking into account the principles for cell-oriented RSFQ design (see [7]). These layouts are designed according to the rules of the 4μm 1kA/cm^2 Nb/Al_2O_3-Al/Nb fabrication technology [15] of PTB-Braunschweig. All RSFQ circuits used for the experimental testing of the library components are fabricated also with this technology and the experiments have been performed at PTB-Braunschweig. A detailed description of the operational principle and the parameters of all gates in the proposed asynchronous RSFQ cell library as well as microphotos of their layouts can be found in [7]. Here, only the gates electrical schemes are presented. They are classified in three groups:

- cells for SFQ pulse conversion and transmission;
- asynchronous DR RSFQ logic gates;
- cells for RSFQ data storing.

The first group includes some classical circuits for generation, conversion and processing of SFQ pulse streams: the DC/SFQ converter (in Fig. 2a), the asynchronous SFQ pulse generator (in Fig. 2b), the SFQ/DC converter (in Fig. 2c), the RSFQ splitter (in Fig. 3a) and the RSFQ merger (in Fig. 3b). The electrical schemes of these five circuits are well known from the literature [3], but here they have been redesigned and optimized [7], [16] for fabrication with the SIS technology of PTB-Braunschweig [15]. Other important gates

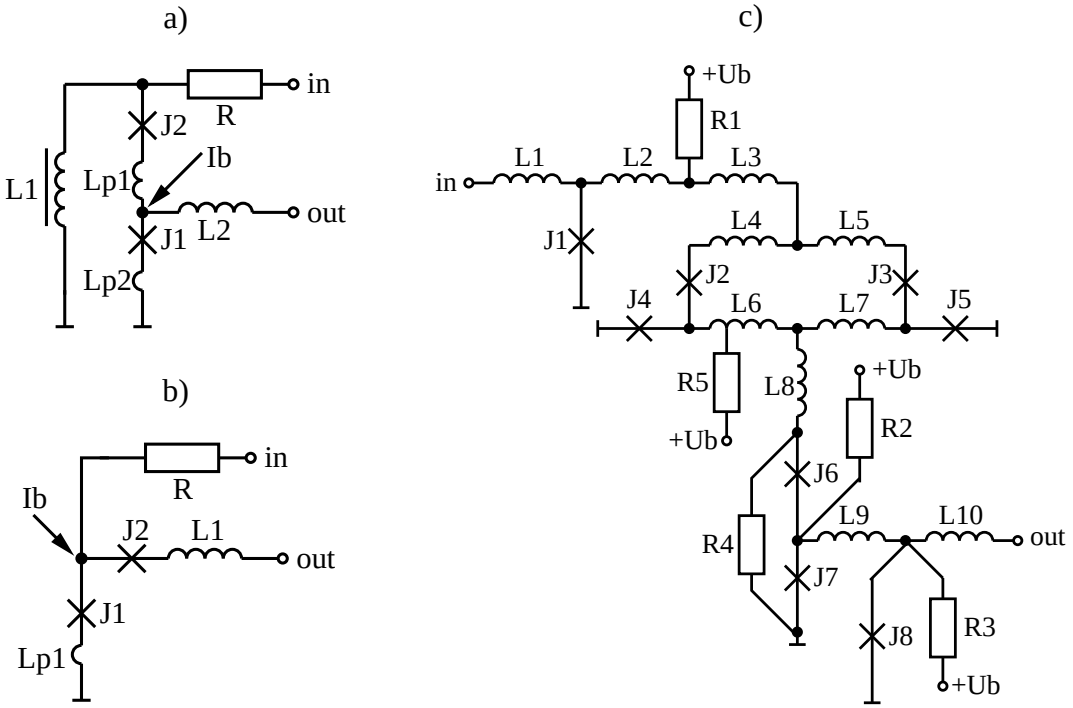

Figure 2. Electrical schemes of the a) - DC/SFQ converter, b) - asynchronous SFQ pulse generator and c) - SFQ/DC converter.

from this group are the Josephson Transmission Line (JTL) and the drivers and the receivers, enabling the SFQ signal exchange via Passive Transmission Lines (PTLs). Currently, the JTLs and the PTLs are the only techniques for SFQ pulse propagation within the RSFQ chips. The JTL is the oldest and the most robust RSFQ circuit [3]. Initially, it was designed and used only to transmit SFQ pulses, later other applications like SFQ pulse shaping, impedance

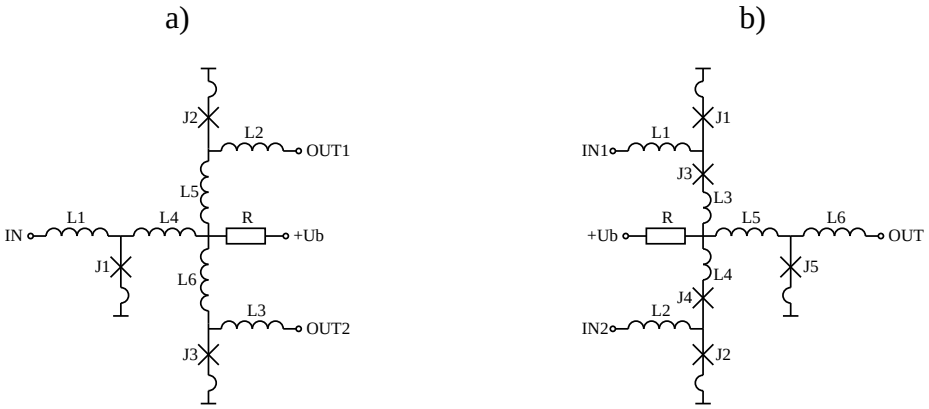

Figure 3. Electrical schemes of a) - RSFQ splitter and b) - RSFQ merger.

matching, delay unit realization, changing of the pulse propagation direction, etc., became actual. Its electrical scheme is shown in Fig. 4 in the classical case of identical Josephson junctions, having critical currents I_c, biased by identical dc bias currents I_b and connected by identical inductances $L1 = L2 = ... = Ln = L$. The basic parameter of the JTL, defining its

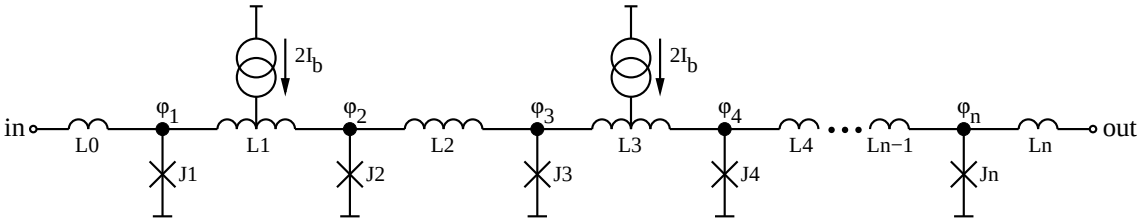

Figure 4. Electrical scheme of a JTL.

dynamic behaviour, is $\beta_L = \frac{LI_c}{\Phi_0}$ ($\Phi_0 = 2.07\text{mV}\cdot\text{ps}$ - the single flux quantum). The established design rules postulate $\beta_L \approx 0.5$ due to the best SFQ pulse shaping and other optimal energy considerations around that point [3], [13]. This is not the optimal value with respect to the SFQ pulse propagation speed of the JTL. In [17] is demonstrated, that the maximum of this speed is reached at values of $\beta_L \approx 1.25$. JTLs with such enlarged connecting inductances also consume less dc bias current and have acceptable margins and fabrication yield. Thus, two of the main drawbacks of the JTLs, restricting their application within the complex RSFQ digital circuits, are significantly improved.

Compared to the JTLs, the PTLs have three big advantages - they are purely passive elements (i.e. have no dc bias consumption); they have significantly higher (up to 10 times) SFQ pulse propagation speed and they have no time-domain instability due to fabrication process deviations. The main drawback, restricting the PTLs straightforward implementation within the RSFQ technique, is their bad matching to the RSFQ circuits. Therefore, PTL drivers and receivers should be put as buffers between the PTL and the RSFQ gates. In the cell library, presented here, they are realized as separate 2-stage gates (see Fig. 5). In this way, the matching of the PTL with **any** RSFQ circuit is ensured [18].

The layouts of the RSFQ gates, described up to now, have been given for fabrication with the SIS technology [15] of PTB-Braunschweig. All of them, except the PTL driver and receiver, have been realized and successfully tested during the experiments, described in [19] and [20]. The fabrication of the chips for testing of the PTL driver and receiver is not yet finished.

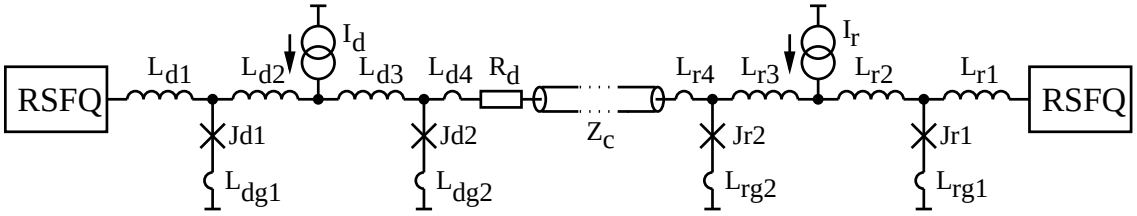

Figure 5. Topologies of the RSFQ driver and receiver, performing the matching between the RSFQ gates and the PTLs. Z_c - the characteristic impedance of the PTL.

The second group of cells includes five novel fundamental asynchronous RSFQ logic gates based on the DR data coding. These are the DR AND, the DR XOR, the DR demultiplexer, the DR multiplexer and the DR Muller C-element. Their electrical schemes are shown in Fig. 6-8. Schemes of the first three gates are presented in [21], but the proposals here have simplified structures. Their first versions are presented in [10], later layouts of the structures have been designed according to the rules of the SIS fabrication technology [15] of PTB-Braunschweig. Exactly these technology-oriented versions of the circuits are included in the asynchronous RSFQ cell library [7]. They have the same topologies as in [10], but other element values. The other two gates (the DR multiplexer and the DR Muller C-element) have not been presented since now.

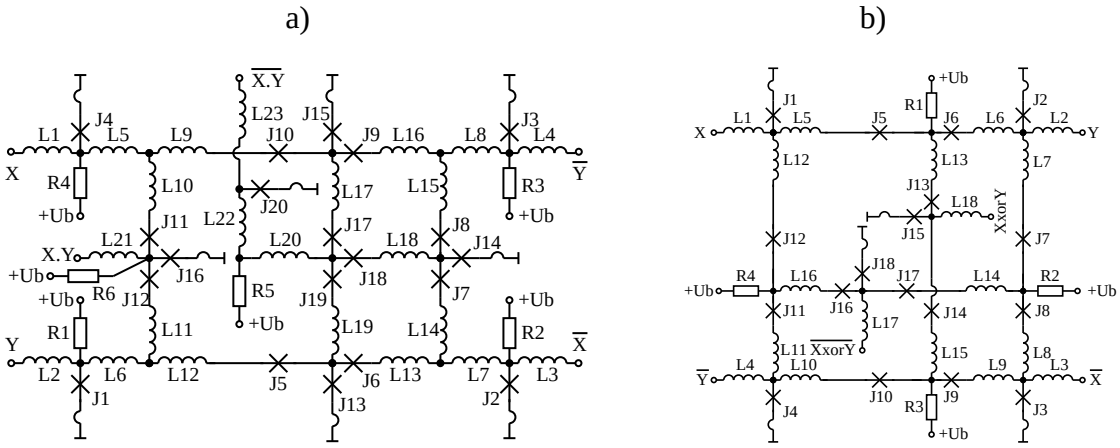

Figure 6. Electrical schemes of a) - DR RSFQ AND gate and b) - DR RSFQ XOR gate.

As described in [21], the DR AND gate can be used also as a DR OR, a DR NAND and a DR NOR. For this, only a simple twisting of its inputs and/or outputs is necessary. Thus, the gates in Fig. 6 cover **all** boolean operations over a pair of DR variables. The DR 2×1 multiplexer and the DR 1×2 demultiplexer (see Fig. 7) can be used to construct $2^n \times 1$ multiplexer and 1×2^n demultiplexer, respectively ($n = 2, 3, \ldots$). For this, $2^n - 1$ such gates should be connected in a tree-shaped network, as demonstrated in [21]. In this way, the communication of the high-speed RSFQ logic with low-speed interfaces is enabled. The DR Muller C-element in Fig. 8 is a key component by the DI synthesis of DR asynchronous circuits. Staying between each pair of communicating DR gates, the Muller C-element guarantees their successful data exchange for any time-domain distribution of the SFQ data.

The three methods for tuning the RSFQ gate delays, described in Section 2.2. of this report, have been applied about the five novel DR gates presented here. Their effectiveness and impact over the gate margins are studied by simulations of the gates electrical schemes. The obtained results are presented in [10] and [7]. In all cases studied, the β_c-method is found

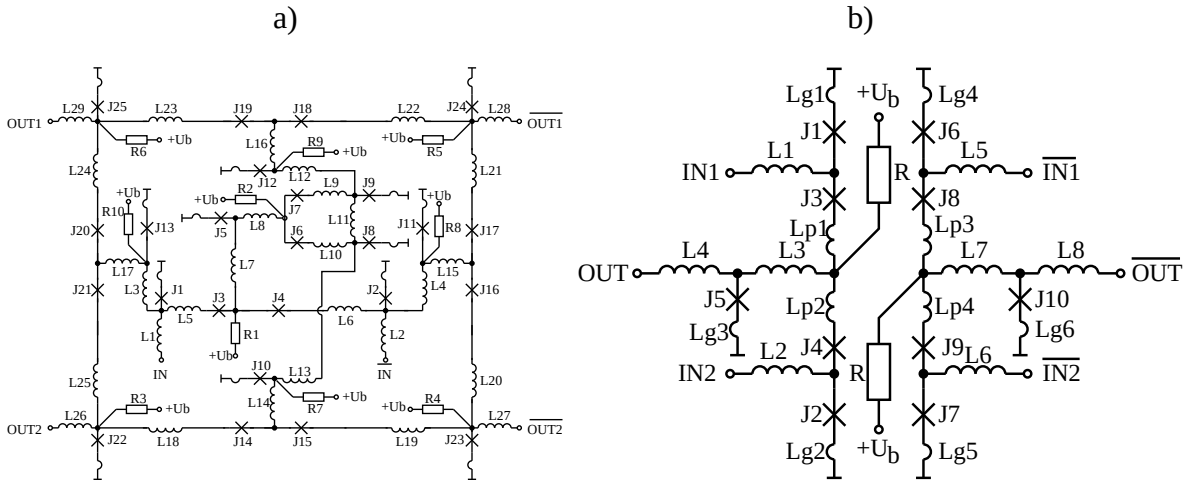

Figure 7. Electrical scheme of a) - 1×2 DR RSFQ demultiplexer; b) - 2×1 DR RSFQ multiplexer.

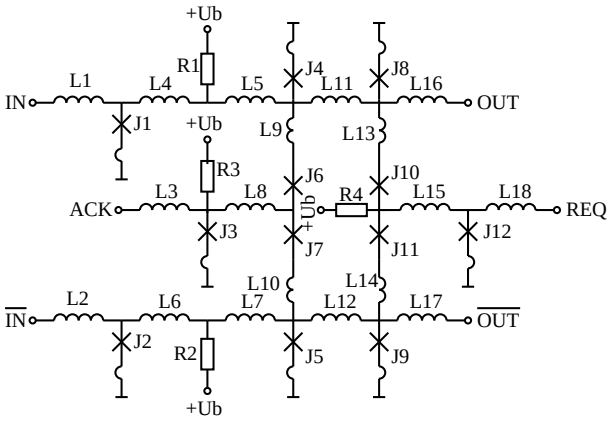

Figure 8. Electrical scheme of a DR RSFQ Muller C-element.

to have a high effectiveness, but negligible impact on the gate margins.

The layouts of the most complex novel DR RSFQ gates - the DR AND, the DR XOR and the DR 1×2 demultiplexer - have been incorporated into RSFQ circuits for their low-speed testing. The measuring concept, implemented in these test circuits, is detailly described in [20]. Remarkable is the number of Josephson junctions, included in the test circuits - 96, 94 and 111 in the case of testing of the DR AND, the DR XOR and the DR 1×2 demultiplexer, respectively. The circuit for testing of the DR AND gate has been successfully measured and the obtained gate's dc bias current margins of ±23% coincide excellently with the predicted by simulations margins of -25%...+19%. The same is true about the test circuit of the DR 1×2 demultiplexer, but the obtained gate's dc bias current margins of ±10% deviate from the predicted margins of ±15%, probably due to technology parameter spread within this chip. An operation of the test circuit of the DR XOR gate has not been obtained due to a design error in the JTL, terminating one of the gate's outputs. A corrected version of this test circuit is being currently fabricated at PTB-Braunschweig.

One of the performance limiting factors of any computation electronic device is its memory. The few RSFQ Random Access Memories (RAMs), reported up to now [22], [23], have complicated structures and big physical dimensions of the circuitry per bit. This problem has motivated the designers to search extensively for more compact and robust RSFQ data

storage circuits and one of the best candidates for this are the RSFQ shift registers. Three different types of RSFQ shift registers have been designed and included into the RSFQ cell library, presented here - the reversible buffered RSFQ shift register, the DR reversible buffered RSFQ shift register and the two-directional buffered RSFQ shift register. Their electrical schemes and operational principles are described in [24].

The reversible buffered RSFQ shift register has the simplest structure and is suitable for synchronous applications, when an unidirectional data propagation is required. It can be included also in asynchronous circuits based on a DR coding, as demonstrated in [24], but can not distinguish between an empty codeword and a ”0” bit. If empty codewords should be stored, the DR reversible buffered RSFQ shift register should be used. It also supports only an unidirectional data propagation. If actual shift-left and shift-right operations should be enabled, the two-directional buffered RSFQ shift register is necessary. Its functionality fully covers the one of the reversible buffered RSFQ shift register, but its elementary cell contains significantly more Josephson junctions.

An important issue considered in [24] is the dependence of the global margins of the shift registers on the data stream speed. The margins are not only decreased with the increase of the data stream speed, but also their optimum point is shifted. In case of synchronous design, the latter is not important - the synchronous circuits are optimized for their nominal clock frequencies and their behaviour at other clock frequencies is not considered. In the case of asynchronous logic, there is generally no fixed time-domain relations between the switching events and the asynchronous circuit should have optimal margins for any speeds of the input data. The development of such an optimization strategy is an open problem requiring a further research.

Up to now, the layouts of the RSFQ shift registers, described here, have not been fabricated. Currently, a circuit for testing of the reversible buffered RSFQ shift register is being fabricated at PTB-Braunschweig.

2.4. Summary and Estimation of the Obtained Results

(i) The asynchronous RSFQ digital circuits are found to be able to overcome the problems, currently restricting the progress of the high-integrated semiconductor devices. Therefore, a concept for the implementation of the asynchronous logic approach within the RSFQ technique has been developed. This concept is based on the dual-rail coding of the binary data;

(ii) An important novel idea of this concept, revealing a new possibility for performance improvement of the complex asynchronous RSFQ circuits, is their speed optimization by tuning the delays of their gates. Three different methods for manipulating the delays of the RSFQ gates have been firstly proposed and compared;

(iii) It has been proven both by simulations and by experiments, that in the case of fabrication technology, based on externally shunted Josephson junctions, the scaling of the junctions external shunts is the best method for manipulating the RSFQ gate delays, because this method has high effectiveness, but does not deteriorate the gate performance. The method is applicable also about the synchronous RSFQ circuits, revealing a new very promising opportunity for improvement of their speed;

(iv) Using the concept for development of asynchronous RSFQ digital circuits, presented here, a cell library has been developed, based on the dual-rail data coding and containing all RSFQ gates, necessary for the high-level synthesis of complex asynchronous RSFQ digital circuits. The layouts of these gates are designed according to the rules of the 4μm 1kA/cm^2 Nb/Al_2O_3-Al/Nb fabrication technology of PTB-Braunschweig;

(v) In order to verify experimentally the functionality of the proposed asynchronous RSFQ gates, a special measuring concept has been developed for their low-speed testing. Test circuits, subjected to this concept, are designed, fabricated and successfully measured about the most complex dual-rail gates of the RSFQ cell library. In this way, the proposed concept for asynchronous RSFQ design has been experimentally proven. Thus, the RSFQ cell library presented here is one of the few RSFQ cell library reported on worldwide, and is the first one, implementing the asynchronous logic approach;

(vi) Due to their complicated structure, some of the proposed asynchronous dual-rail RSFQ logic gates have relatively narrow margins, i.e. a reliable complex asynchronous circuits with enough high fabrication yield can be produced only with a stable and exact fabrication technology;

(vii) One of the most valuable results from the present work is the very good agreement between simulated and measured data, obtained during all experiments within this project. This agreement proves the exactness of the used techniques for RSFQ design, which is an important and fundamental precondition for the successful realization of any kind of RSFQ digital devices.

2.5. Possible Applications of the Obtained Results

The RSFQ electronics is an emerging technique and has few commercial applications, mostly within the telecommunications for building of ultra-fast commutation devices (switches). Exactly in this case the application of the asynchronous approach is quite promising and has been often applied, because the communication of high-speed data rates between distant points imposes very hard, mostly unsolvable restrictions over the global synchronization. Nevertheless, the low-level design of complex purely asynchronous RSFQ digital devices meets hard problems with the circuit synthesis, simulation and testing and the only possibility for their efficient, facilitated and reliable design is given by the cell-oriented approach. The proposed concept about the implementation of the asynchronous approach within the RSFQ technique and the complete asynchronous RSFQ cell library for high-level synthesis of complex asynchronous RSFQ digital devices are an important step towards such a design.

2.6. Open Problems for Further Research

(i) A concept should be developed about the high-level speed optimization of complex asynchronous circuits by adjusting the delays of their gates;

(ii) The existing techniques for optimization of synchronous circuits should be modified and extended about the case of asynchronous logic optimization.

2.7. Project Co-workers and Cooperators

The theoretical studies and the RSFQ circuit designs reported on here are performed by Dipl.-Ing. Boyko Dimov, who has occupied the scientific co-worker position within this project. During the test circuits designs, he has used the SFQ/DC converter, designed by Dipl.-Ing. Jörn Weber during his Master thesis preparation (see Section 2.8. of this report).

The circuits fabrication has been performed within the project collaboration with the colleagues from the RSFQ division of PTB-Braunschweig (DFG research project Ni253/3-3). The measurements of the fabricated circuits have been performed also there.

2.8. Scientific Qualifications Connected to This Project

Students works:

- A. Fell, "Untersuchung supraleitender Einzelflussquantenschaltungen," *Fakultät für Elektrotechnik und Informationstechnik, Institut für Allgemeine und Theoretische Elektrotechnik, TU Ilmenau,* 2004
- A. Frommhold, "Dynamische Analyse einer universellen asynchronen Logikschaltung in Einzelflussquantentechnik," *Fakultät für Elektrotechnik und Informationstechnik, Institut für Allgemeine und Theoretische Elektrotechnik, TU Ilmenau,* 2004
- J. Weber, "Untersuchung zur Realisierung von Grundschaltungen für Quantencomputer," *Fakultät für Elektrotechnik und Informationstechnik, Institut für Allgemeine und Theoretische Elektrotechnik, TU Ilmenau,* 2002

Master thesis:

- J. Weber, "Untersuchung der Schalt- und Verzögerungszeiten einer supraleitenden Hochgeschwindigkeitselektronik im Pikosekunden-Bereich," *Fakultät für Elektrotechnik und Informationstechnik, Institut für Allgemeine und Theoretische Elektrotechnik, TU Ilmenau,* 2003

PhD thesis:

- B. Dimov, "General Restrictions and Their Possible Solutions for the Development of Ultra High-Speed Integrated RSFQ Digital Circuits," *eingereicht an der Fakultät für Elektortechnik und Informationstechnik der TU Ilmenau am 01.11.2004,* wiss. Betreuer: Prof. Dr.-Ing. habil. F. H. Uhlmann

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3. Zusammenfassung

With its picosecond switching times and extremely low power consumption, the LTS RSFQ technique is a promising alternative to the modern semiconductors for the development of ultra high-speed digital devices. There are plenty of successfully reported simple LTS RSFQ circuits, operating at multigigahertz clock frequencies, but if the complexity of the LTS RSFQ digital device is raised up to even several thousands of Josephson junctions, the clock frequency falls drastically down to several tens GHz. One of the reasons for this big gap, which has also motivated the present research, are the problems, originating from the global synchronization of ultra high-speed complex digital circuits. Within this project, a concept about the implementation of the asynchronous approach within the RSFQ technique has been developed together with a complete asynchronous RSFQ cell library, based on this concept and supporting the high-level synthesis of complex asynchronous RSFQ digital devices.

The milestones of the work within this project are:

- Improving of the existing techniques for on-chip SFQ pulse transmission - these are: via JTLs and via PTLs. Having serious drawbacks, both approaches impose significant restrictions about the signal exchange within the LTS RSFQ digital circuits. New design approaches, improving these drawbacks, have been developed;
- Investigation of the possible methods for speed optimization of the asynchronous RSFQ digital circuits by tuning of the delays of their gates - three such methods are here proposed, compared and evaluated and the β_c-method is estimated as the best one. It has been demonstrated, that one can apply this method without taking cares about a possible degradation of the performance of the optimized RSFQ gates;
- Design of a cell library, containing all RSFQ gates, necessary for the high-level synthesis of asynchronous RSFQ computational devices. The most complex gates have been fabricated and successfully tested. The experimentally obtained results coincide well with the predicted by simulations behaviour of the gates; the minor deviations can be attributed to the spread of the fabrication technology parameters.

A common feature of all asynchronous DR RSFQ gates, described in this report, is their relatively complex structure, resulting into relatively narrow margins and high sensitivity to the parasitic inductances between the Josephson junctions and ground. Thus, the conclusion is drawn, that a reasonable fabrication yield of a complex DR RSFQ circuit can be achieved only with a stable fabrication technology, providing reduced junctions parasitics.

Another feature, characterizing the asynchronous DR RSFQ gates, is the increased (in comparison to their synchronous equivalents) number of signal ports. Due to this fact, the ports termination with JTLs or other RSFQ gates is often geometrically impossible or results in large structures, unacceptable in the case of high-speed densely-packaged RSFQ designs. Therefore, the PTLs are estimated as the only reasonable type of interconnects, which should be used within the complex asynchronous RSFQ circuits based on the DR data coding. The universal PTL drivers and receivers proposed here are able to match only PTLs with large lateral dimensions. The invention of efficient techniques for direct matching between compact PTLs and the DR RSFQ gates is a vital precondition for the realization of successful high-speed and high-integrated asynchronous RSFQ digital devices.

Finally, the very good agreement between simulated and measured data, obtained during all experiments connected to this project, should be pointed out once again. This proves experimentally the exactness of the design approach, used here. The latter is estimated as one of the most valuable results, coming out from this work, because the availability of exact techniques for modeling, simulation and optimization is the most fundamental precondition for successful design of any kind of digital circuits.